Continuous Time Sigma Delta Modulator Employing a Novel Comparator Architecture

Vijay U.K. 
CEDT Dept., IISc, Bangalore. 
viju221@yahoo.co.in

Amrutur Bharadwaj 
ECE Dept., IISc, Bangalore. 
amrutur@ece.iisc.ernet.in

Abstract

A novel comparator architecture is proposed for high speed operation in low voltage environment. Performance comparison with a conventional regenerative comparator shows a speed-up of 41%. The proposed comparator is embedded in a continuous time Sigma-delta ADC so as to reduce the quantizer delay and hence minimizes the excess loop delay problem. A performance enhancement of 1dB in the dynamic range of the ADC is achieved with this new comparator. We have implemented this ADC in a standard single-poly 8-Metal 0.13µm UMC process. The entire system operates at 1.2V supply providing a dynamic range of 32dB consuming 720µW of power and occupies an area of 0.1mm².

1. Introduction

The advancement in CMOS process technology due to scaling has led to digital circuits gaining more advantage than the Analog counterpart. Hence the current trend is to replace analog signal processing with low power digital signal processing. One of the approaches towards this is the emerging Low-IF transceivers where the base-band processing is done in digital domain with the analog to digital converter meant to digitize the signals located at IF. The low power implementation of these transceivers has led to the realization of various personal area networks. One of the most recent and promising wireless personal area network (WPAN) technologies is the IEEE 802.15.4 (Zigbee standard) [1]. For Low-IF transceivers compliant to Zigbee standard, the intermediate frequency where the signal is located can range from kHz to few MHz depending on the transceiver design. Hence the analog to digital converter used in these transceivers should cater for low power and high speed requirements at acceptable linearity.

In this paper, we report a second order continuous time Sigma-delta ADC intended to be used in the Low-IF transceivers compliant to Zigbee standard. Various non-idealities such as excess loop delay, clock jitter etc. [2] affects the performance of continuous time Sigma-delta modulator. The effect of clock jitter is minimized by choosing Non-Return to Zero (NRZ) pulse shaping of the digital to analog converter (DAC) in the modulator [3]. In order to minimize the excess loop delay problem, one of the viable solutions is to reduce the delay of the loop comprising of the Quantizer and the DAC. This is accomplished with the help of a high speed comparator embedded in the quantizer in order to reduce the quantizer delay. The excess loop delay problem is analyzed using behavioural simulations in MATLAB (Simulink). The performance comparison of the proposed comparator is made with a conventional regenerative comparator. The overall performance enhancement with the use of proposed comparator in the Sigma-delta ADC is determined.

Section 2 of this paper provides a brief discussion on the excess loop delay problem. Section 3 provides the details of the circuit implementation. Section 4 describes the conventional and proposed comparator architectures. Section 5 lists the simulation results and Section 6 concludes this paper.

2. Excess Loop Delay

The architecture of the Sigma-delta modulator is shown in Figure 1 [3]. The “ωs/s” block implements the integrator transfer function with ωs = (2*π*Fs), where F_s (=160MHz) is the sampling frequency and “a1”, “a2”, “a3”, “a4” are the loop coefficients. The Noise transfer function for discrete time Sigma-delta modulator is obtained from Scherier MATLAB Toolbox [4]. It is then transformed to continuous time domain using bilinear transformation and the corresponding loop coefficients (Figure 1) are derived.
The active integrators integrate the continuous time signal which is the subtracted version of the input signal and the feedback signal. Ideally the feedback delay should be zero. But due to inherent delay of MOS transistor circuits, the feedback signals arriving at the integrator’s input summing junction gets delayed and hence degrades the SNR.

Figure 2. Excess loop delay effects

The effect of this delay (known as Excess loop delay) is studied using behavioural MATLAB simulations by varying the feedback delays independently and determining their effect on the SNR. The result is plotted in Figure 2 which shows the SNR plot versus the delay in the two feedback branches of the Sigma-delta modulator. DELAY-1 and DELAY-2 corresponds to the feed-back signal delay to the input of the first and second integrator respectively.

From Figure 2, it is clear that the effect of the delay is more critical at the input summing junction of the second integrator than that at the first integrator. This is because, the degradation of the SNR occurs mainly due to saturation of output of the second integrator. Hence the feedback delay to the second integrator input is more crucial. On the other hand, if the feedback to the first integrator input is delayed while the feedback signal delay to the input of the second integrator (DELAY - 2) is smaller, then the second integrator is able to track the output of the first integrator and the loop stabilizes. From Figure 2, we observe that when the loop delay (both DELAY - 1 and DELAY - 2) is within 10% of the clock period, it doesn’t cause much degradation of SNR. Hence the design target is to maintain the total feedback delay within 10% of the clock cycle (i.e. 625ps for 160MHz clock frequency).

3. Circuit implementation

The block diagram of the second order continuous time Sigma-delta modulator is shown in Figure 3 [3]. It consists of Integrators, Quantizer and Digital to Analog converters (DAC 1 and DAC 2).

3.1. Integrators

Opamp-RC integrators provide good linearity when compared to Gm-C or MOSFET-C integrators as the passive resistors are inherently linear [2]. Hence the integrators are implemented using Opamp-RC configuration. Resistor calibration is employed in the Opamp-RC integrators to compensate for resistance and capacitance variations across corners. Two stage miller compensated Opamp with resistive common mode feedback (CMFB) [5] is used in the Opamp-RC integrators. Low Vth PMOS transistors are used as input devices to overcome swing limitations. The Opamp is observed to scale with power supply with the DC gain maintained at 60dB upto 800mV of supply voltage.

3.2. Quantizer and DAC

The Single bit quantizer is implemented using a clocked comparator followed by SRAM latch circuitry. The decision made by the comparator at the rising edge of the clock is latched for one full clock cycle by SRAM latch circuitry [5].

Differential current steering DAC is employed [6]. The delay of the DAC is very small as current switching is employed. Hence the feedback path delay is dominated by the quantizer delay which is reduced by the proposed comparator circuit as discussed in the following section.
4. Comparator

The comparators used for Sigma-delta A/D converters normally employ input transistors and the cross-coupled load transistors in a single stage as shown in Figure 4 [7]. It consists of input transistors (M2 and M3) and clock transistor (M1). The output is precharged to VDD when clock is low by the precharge transistors (M6 and M9). Transistor M10 provides for equalization between the two input branches.

The latching process of the comparator can be divided into two phases. In the first phase, both the output nodes fall to about half the supply rail with a slight voltage imbalance created due to the input differential. In the second phase, output regenerates to rail to rail value. In order to speed up both phases, the discharge path delay should be reduced. From Figure 4 we find that there is stacking of transistors one above the other (M1, M2, M4) which in turn increases the delay of the discharge path. The stacking also reduces the effective gate overdrive of the input transistors thus reducing their transconductance. All these drawbacks results in increase in the delay of the comparator and thereby affecting the loop delay.

The circuit can be speeded up by shifting the input transistors below the clock transistors as shown in Figure 5. This eliminates the threshold voltage increase due to body effect of the input transistors and also provides larger gate overdrive across the input transistors. The transistors in the output discharge path were upsized in order to decrease their resistance and increase the speed at the cost of increased power consumption. But there was an optimum point beyond which the internal node capacitance dominates and starts degrading the circuit performance.

In order to further speed up the comparator circuit, we add a separate regenerative branch along with the input branch as shown in Figure 6. The main idea is to reduce the stacking effect by separating the input branch and the regenerative branch of the comparator. When Clock is low, the outputs of the comparator are precharged by the precharge transistors (M7, M10). Transistors M3 and M4 ensure that the input branch remains turned off when the clock signal is low. At the rising edge of the clock, the input branch and the regenerative branch are activated. The regenerative branch enables both the output nodes to fall to about half the supply voltage at a faster rate. Once the output nodes are at mid-supply rail, the parallel paths provided by the input branch and the regenerative branch assist in output regeneration.
Figure 5. Improved conventional comparator

The cross-coupled transistors M12 and M13 in the regenerative branch are closer to the output nodes as opposed to having cascode transistors separating them from the output nodes as in [8]. This ensures an overdrive voltage equal to the supply voltage appearing across the transistors M12 and M13 at the time of output regeneration i.e. \((V_{GS} - V_{th})_{M12, M13} \sim V_{DD}\) since the output nodes are precharged to \(V_{DD}\). This in turn increases the speed of the regenerative branch. In order to achieve high resolution, the intermediate nodes of the comparator should be equalized so that the residual charge from the previous comparison cycle is removed at these nodes. Transistors M7 and M10 precharge output nodes of the comparator (OUT+ and OUT- in Figure 6) whereas transistor M11 equalizes the drain nodes of M3 and M4.

5. Simulation results

The Sigma-delta modulator is implemented in UMC 0.13\(\mu\)m Mixed-mode RF-CMOS process and is simulated using Spectre simulator of Cadence.

5.1. Quantizer

The Quantizer is characterized using both the conventional and proposed comparator circuits. The input voltage switches from rail to rail swing to a differential voltage swing of 2\(\mu\)V peak before the rising edge of the clock signal. Table 1 shows the comparison results obtained from schematic simulation using Cadence Spectre simulator.

Figure 6. Proposed comparator

We find that there is an improvement of 41% in the propagation delay of the quantizer using the proposed comparator in the typical process corner. The fall time of the proposed comparator is higher than that of the conventional architecture. This is because during the output regeneration since the output nodes are pulled down by the regenerative branch, the falling edge begins to fall earlier thereby increasing the fall time. The power dissipation is higher compared to conventional architecture as proposed comparator architecture uses an additional regenerative branch.

Figure 7 shows the delay variations of Quantizer with supply voltage scaling for an input differential of 2\(\mu\)V. We find that the proposed architecture scales better with supply voltage working up to a power supply voltage of 0.5V. This is due to sufficient overdrive voltage across cross-coupled transistors M12 and M13 in Figure 6 which ensures output regeneration at low supply voltage.

5.2. Layout

The layout of the Sigma-delta modulator is shown in Figure 8. All transistors, resistors and capacitors that are bounded by stringent matching constraints are implemented using common centroid configuration. Sufficient guard rings are provided for isolation between Analog and digital blocks. The Clock signal is isolated from other signals by providing ground lines surrounding the clock signal line. The layout is floor planned such that the length of the feedback path is reduced.
Table 1. Schematic results of the Quantizer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Conventional</td>
<td>Improved</td>
<td>Proposed</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>Rising</td>
<td>Rising</td>
<td>Rising</td>
</tr>
<tr>
<td>Typical Corner</td>
<td>326 ps</td>
<td>223 ps</td>
<td>193 ps</td>
</tr>
<tr>
<td>Slow Corner</td>
<td>516 ps</td>
<td>408 ps</td>
<td>364 ps</td>
</tr>
<tr>
<td>Rise/ Fall time</td>
<td>Rise Time</td>
<td>Rise Time</td>
<td>Rise Time</td>
</tr>
<tr>
<td>(Typical Corner)</td>
<td>65.5 ps</td>
<td>67 ps</td>
<td>66 ps</td>
</tr>
<tr>
<td></td>
<td>Falling Time</td>
<td>Fall Time</td>
<td>Fall Time</td>
</tr>
<tr>
<td></td>
<td>282 ps</td>
<td>62.3 ps</td>
<td>82 ps</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>14 μW</td>
<td>15.5 μW</td>
<td>19 μW</td>
</tr>
</tbody>
</table>

Table 2. Layout extracted results of the Quantizer

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation Delay</td>
<td>Rising edge</td>
</tr>
<tr>
<td></td>
<td>230 ps</td>
</tr>
<tr>
<td></td>
<td>Falling edge</td>
</tr>
<tr>
<td></td>
<td>165 ps</td>
</tr>
<tr>
<td>Offset</td>
<td>21 mV</td>
</tr>
<tr>
<td>Rise/ Fall time</td>
<td>Rise Time</td>
</tr>
<tr>
<td></td>
<td>98 ps</td>
</tr>
<tr>
<td></td>
<td>Fall Time</td>
</tr>
<tr>
<td></td>
<td>94 ps</td>
</tr>
</tbody>
</table>

The layout extracted parasitic results of the Quantizer with the proposed comparator circuit shows a positive offset of 21 mV (Table 2). This is due to two reasons. First one is that, an error was made by not including the equalization transistor M11 (Figure 6) in the taped out version of the proposed comparator circuit in the test chip. Transistor M11 helps to remove residual voltage difference from the previous cycle and hence is crucial for achieving a low offset. A second smaller source of offset is an asymmetry in signal routing in the layout of the Quantizer.

Figure 9 compares the schematic results of the designed ADC using the new comparator architecture (Figure 6) with the conventional architecture employing regenerative comparator (Figure 4). An overall improvement of 1 dB is observed in the dynamic range. This is due to reduction in the loop delay facilitated by the high speed comparator. The improvement occurs at the higher end where the signal amplitude is larger as the offset of the proposed comparator dominates for low amplitude input signals.

Figure 7. Supply voltage scaling

Figure 8. Layout of Sigma-delta modulator
5.3. Sigma-delta ADC

The Figure of Merit, \( FOM = \frac{P}{2^{\text{ENOB}} \times F_B} \)
where \( F_B \) = Signal bandwidth, \( P \) = Power consumption, \( \text{ENOB} \) = Effective Number of Bits. Figure 10 plots the FOM of the implemented ADC as compared to other ADCs in literature. It is observed that the performance of the implemented Sigma-delta converter is comparable to the performance of other ADCs.

![ADC COMPARISON](image)

Figure 10. FOM comparison

Table 3 lists the performance summary of the Sigma-delta modulator.

6. Conclusion

The challenges in implementing a continuous time Sigma-delta modulator in a low voltage deep sub-micrometer CMOS process have been explored. A novel comparator architecture is proposed in order to reduce the excess loop delay problem in continuous time Sigma-delta modulator. The proposed comparator is also observed to scale better with the supply voltage. The comparator shows an improvement of 41% in the propagation delay when compared to a conventional comparator and works up to 500mV of supply voltage in a 0.13\( \mu \)m process. An overall improvement of 1dB is observed in the dynamic range of the Sigma-delta modulator using this new comparator.

7. Acknowledgements

We are thankful to Cadence Inc. for extending the license and DRDO for the Project support. We thank Cosmic Circuits for reviewing the design. We also thank Pratap kumar Das, Sudhir kudva, Jagdish Pandey for their involvement and helpful discussions.

8. References


