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Multiphase technique to speed-up delay measurement via sub-sampling

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***Abstract*—A multi-phase technique for speeding up the measurement of delays via sub-sampling is presented. Measurement of delays using the sub-sampling approach leads to a very simple system implementation, and also provides the opportunity of trading off between bandwidth and accuracy. Such a scheme becomes extremely attractive for deep sub-micron processes due to its highly-digital nature and the ability to offer compact, low power, mixed-signal implementation alternatives. However, a drawback is the amount of averaging (measurement time) that is needed to get accurate results. A multiphase input clock scheme is proposed to address this issue, especially for the measurement of small delays, thereby speeding up the overall measurement. Simulation results from MATLAB Simulink confirm the speedup achieved upto a factor of eight with an eight-phase clock input for sufficiently small fixed test delays and also an improvement in SNR upto 11dB for slowly varying test delays.**

***Index Terms*—Sub-sampling, Deep sub-micron, mixed-signal**

I. Introduction

The strive for nearly-minimum energy operation is pushing VLSI circuits and systems towards reduced supply voltages. With the increasing popularity of deep-sub-micron CMOS processes, the design of mixed signal circuits is getting increasingly difficult due to reducing supply voltages and increasing process variations. However, in such deep sub-micron (DSM) processes, the time domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals [1]. Hence, a lot of recent research activity has focused on designing ADCs using time-based methods. Design of ADCs using time-to-digital converter (TDC) architectures are described in [2], [3] while that using VCO-based methods are described in [4], [5]. An implementation of temperature sensor using TDC is described in [6]. The design of a digital phase-locked-loop (PLL) using TDC is presented in [7]. A minimally invasive delay slack monitor is presented in [8] that directly measures the timing margins on critical timing signals, allowing timing margins due to PVT and global variations to be removed. A technique of measuring skews between leaf nodes of a clock tree by way of sub-sampling is presented in [9]. An architecture of built-in-self-test (BIST) for measuring low-bandwidth analog signals using the approach of delay measurement is presented in [10]. In essence, accurate delay measurement is becoming important for the implementation of important mixed-signal and sensor blocks in deep-sub-micron processes. Hence, such implementations for measuring delay should consume less power, operate at low supply voltages and be portable to further DSM processes. When information about voltage, temperature, phase or other (analog) quantities is encoded in the delay (between a pair of clocks) or in the frequency (of a clock, as in VCO), the edge transitions of the clock signal/s actually contain the information. Also it is important to minimize the number of such transitions to reduce power consumption.

The basic block diagrams for the different methods of delay measurement mentioned above are shown in Fig. 1. The comparison between them is summarized in Table I. From the entries, it is clear that the resolution of a basic TDC is one inverter delay, and as a result the linearity gets affected by mismatch. A vernier TDC improves the resolution at the cost of reduced dynamic range. A vernier ring TDC reduces the impact of mismatch at the cost of increased measurement time.

An inverter delay (or the difference delay between a pair of inverters) is the minimum delay that can be measured using the TDC-based approaches. Oversample-and-average methods similar to ADCs [11] can be employed, but the test-delays should vary by about an inverter delay across measurements to achieve improvement in resolution by averaging. Test delays smaller than an inverter delay can be amplified as described in [12] and measured using TDC, but the delay-amplifier needs to be calibrated to determine its gain. Instead, sub(Nyquist)-sampling technique can be used to amplify such small test-delays, which also greatly simplifies the implementation of the delay-measurement unit (DMU) that follows [9]. It turns out that the components needed, and thereby the area occupied, is independent of the resolution to be achieved. As the sampling rate is lesser than Nyquist, this technique demands that the delay should be on a periodic signal, a *clock*. Also, this means that the measurement of delays which are small compared to the time-period of clock will need a lot of averaging, which leads to larger measurement time. A technique is proposed in this paper to reduce the measurement time without compromising accuracy, especially for the measurement of small delays.

The organization of the rest of the paper is as follows: Section II describes the problem statement, Section III presents the proposed solution, Section IV presents the simulation results and Section V concludes.

II. Problem Statement

A delay measurement unit based on sub-sampling is presented in [9] (refer Fig. 2), the salient features of which are

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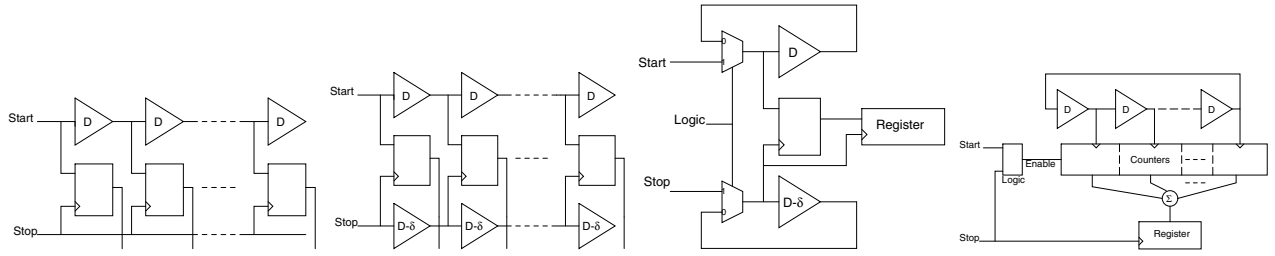

(a) A Basic TDC [2] (b) A Vernier TDC [2] (c) A Vernier Ring TDC (d) VCO based time measurement [5]

Fig. 1. Block diagrams of architectures for time measurement

discussed here to setup the context of the paper. Suppose a delay d is present between a pair of clock signals of period T. This clock pair is sampled by an asynchronous[1] clock of period $T+\Delta T$. Since this sampling frequency is lesser than Nyquist rate, the original signal cannot be fully reconstructed back, but the period of the (sub)sampled signal is $T(T+\Delta T)/\Delta T$; *i.e.*, there is "time amplification" compared to the input clock pair of period T. Fig. 3 shows the timing diagram of the various signals. Hence, the delay d between the clock pair D_a and D_b is also amplified to become $d(T+\Delta T)/\Delta T$ between Q_a and Q_b. Since Q_a and Q_b are synchronous with respect to the sampling clock, the delay between them can be measured using a counter. Q_a and Q_b are illustrated with bouncing edges because of jitter in the clocks and metastability issues of the flip-flops. The falling edges of Q_a and Q_b are made to align so as to extract only the delay on the rising edge. The period

[1]Asynchronous means a clock of different frequency which is not derived from the input clock.

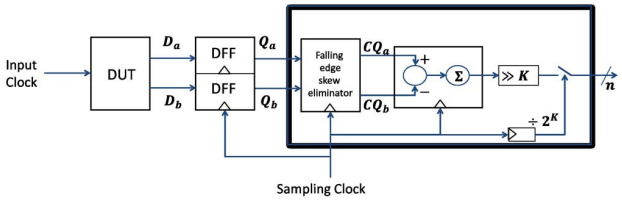

Fig. 2. Block diagram of DMU (Delay Measurement Unit) based on sub-sampling

of the sub-sampled signal is called the beat period and is the least time in which a given delay can be measured.

It is well known that the asynchronous sampling described above leads to the case of random sampling, which is demonstrated in evaluating ADC performance [13] and in calibrating delay between two clock phases [14]. To understand this process of random sampling, let the input clock be modeled as a circle since it is periodic with period T (the circumference

TABLE I
COMPARISON OF VARIOUS TIME MEASUREMENT ARCHITECTURES

Specification	Basic TDC [2]	Vernier TDC [2]	Vernier Ring TDC [2]	VCO-based TDC [5]	DMU based on sub-sampling [9]
Resolution	Inverter delay, D	Inverter difference delay, δ (Fig. 1(b))	Inverter difference delay, δ (Fig. 1(c))	Inverter delay D	Limited by measurement time
Measurement time (for b bits)	2^b inverter delays $\sim 2^bD$	2^bD	$> 2^bD \cdot 2$ (due to circling)	at least 2^bD	$2^b(T+\Delta T)$
Dynamic range available (Ratio of maximum to minimum measurable delays)	$nD/D = n$	$n\delta/\delta = n$	No upper limit on measurable delay	No upper limit on measurable delay	$< T/\sigma$ where σ is the standard deviation of smallest measured delay
Mismatch	LSB directly affected	LSB directly affected	Reduced due to reuse of inverter stages	Reduced due to reuse of inverter stages	Appears as offset which can be calibrated out
Quantity output for an input delay d	$\left\lfloor \frac{d}{D} \right\rfloor$	$\left\lfloor \frac{d}{\delta} \right\rfloor$	$\left\lfloor \frac{d}{\delta} \right\rfloor$	$\left\lfloor \frac{d}{D} \right\rfloor$	$\frac{d}{T}$
Information needed to obtain absolute delay (in ps)	D, average inverter delay	δ, average inverter difference delay	δ, inverter difference delay	D, average inverter delay or Time period of VCO	Time period T
Components required (for b bits)	2^b inverter stages and 2^b flops	2^{b+1} inverter stages and 2^b flops	2 inverter stages, a flop and a counter at frequency of $\frac{1}{2D}$	2^b inverters and a counter at VCO frequency	2 flops and b-bit up/down counter
Nature of measurement	Single-shot	Single-shot	Single-shot	Single-shot	Periodic (requires test delay to be present on a periodic signal)

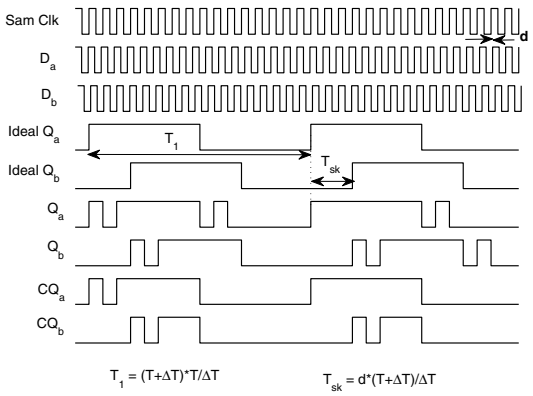

Fig. 3. Timing diagram

corresponding to T). Then, the delay between the clock pair can be modeled as a sector in this circle. Since the time period of the sampling clock is greater than the input clocks, the sampling clock edges precesses around the circle. Please refer Fig. 4. The problem is to estimate the size d of the sector and an estimate is given by:

$$\hat{d} = \frac{\text{No. of points in the sector corresponding to delay}}{\text{Total no. of points corresponding to time-period}} \times T \tag{1}$$

It can be shown that this is an unbiased estimator of the delay and is easy to note that this estimate has least variance if the total number of points span the length of an integer multiple of the circumference [9]. To be able to calculate (1) practically, two counters are needed; one each for delay and time-period counts.

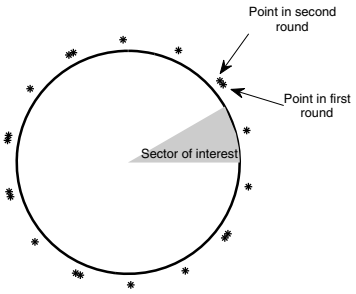

Fig. 4. Illustration of the sampling clock precessing around the input clock. The circumference represents the time period of input clock while the sector represents the delay to be measured. The asterisk shaped points are the edges of sampling clock.

If the delay d is a small fraction of the time period T, then the majority of the sampling points do not contribute to the numerator of (1) limiting the use of such data points. This problem is analogous to the situation of rare events in a Monte-Carlo simulation [15] and to the need of automatic gain control (AGC) in ADCs to prevent its under-utilization. A straight-forward solution is to use high frequency clocks (low T) which makes it consume more power and not work at low supply voltages. Hence, it is interesting to apply techniques similar to rare-event simulation and AGC for quicker delay estimation.

III. Proposed Solution

Consider a toy example where the periods of input clock and sampling clock are 16 and 17 units respectively, with the test delay being 2 units. The duration of a beat period is $16 \times 17 = 272$ unit and the delay is amplified to $2 \times 17 = 34$ unit. As a result, the period counter goes till 16 (= 272/17) and delay counter till 2 (= 34/17); which means that 14 samples out of 16 do not contribute much to delay measurement. If a two-phase clock were available, having detected that the delay counter is not changing, the other phase is fed to the counter. Hence, the delay counter now will count upto 4; but has to be divided by 2 since two-phases were used. Similarly, use of a 4-phase clock will yield a delay count of 8, which needs to be divided by 4 to get the actual delay. Fig. 5 illustrates this example.

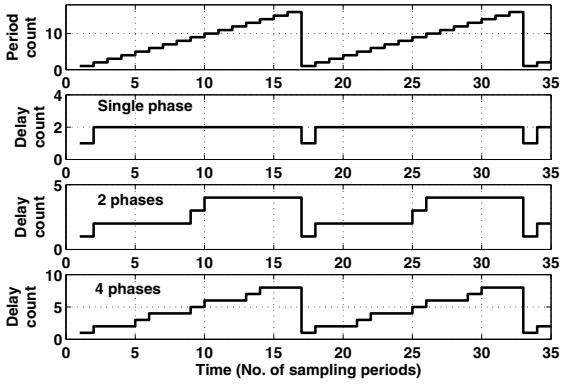

Fig. 5. Counts corresponding to period and delay. Two-phase and four-phase clocks measure delay twice and four times in a beat period respectively, thus providing more accuracy in the same measurement time.

In general, suppose an N-phase clock is available and we are interested in measuring the delay of a DUT (Device Under Test). At the end of the first beat period, the counts for the delay and time-period will be available. In each of the subsequent beat periods, once the delay count saturates, the next appropriate phase is calculated and fed to the DUT. As a result, the sector of interest is scanned multiple times in a beat period, leading to reduced measurement time for same accuracy or improved accuracy for the same measurement time. The flowchart describing this process is shown in Fig. 7.

An issue, though, is that the phase spacings of the N-phases may not be equal. Let $\phi_1, \ldots, \phi_N$ be the phases and let $d_1^i, \ldots, d_n^i$ and $p_1^i, \ldots, p_n^i$ be the counts of delay and period respectively for each phase in the i^{th} beat period (Here $n < N$ since all the available phases may not be used). We need an estimate for the delay d based on $d_1^i, \ldots, d_n^i$ and $p_1^i, \ldots, p_n^i$.

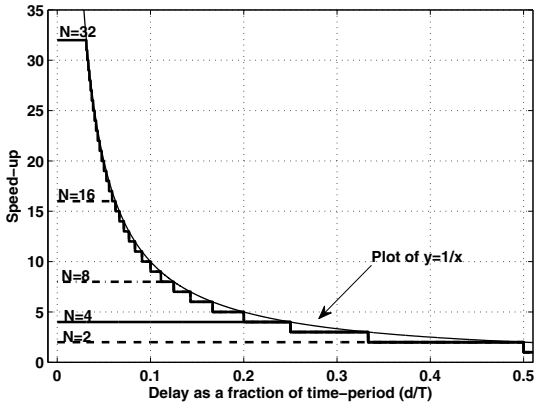

Fig. 6. Plot of speed-up obtained corresponding to fraction of delay to time-period. Here N is the number of phases of clock available.

One possibility is to use

$$\hat{d} = \left(\frac{d_1^i}{p_1^i} + \cdots + \frac{d_n^i}{p_n^i} \right) \times \frac{T}{n} \tag{2}$$

This estimate is not accurate since the counts $p_1^i, \ldots, p_n^i$ can be different due to unequal phase-spacings. A better estimate is given by:

$$\begin{aligned} \hat{d} &= \frac{d_1^i + \cdots + d_n^i}{p_1^i + \cdots + p_n^i} \times \frac{T}{n} \\ &= \frac{d^i}{p^i} \times \frac{T}{n} \end{aligned} \tag{3}$$

where $d^i = d_1^i + \cdots + d_n^i$ and $p^i = p_1^i + \cdots + p_n^i$. Estimate of (3) is better since the sum of all phase-spacings is very close to an integer multiple of the time period modulo the jitter. The speed-up of this scheme over the single phase case is given by:

$$\text{Speed} - \text{up}, n = \min \left(N, \left\lfloor \frac{T}{d} \right\rfloor \right) \tag{4}$$

The plot of speed-up n versus the delay (d as a fraction of time-period T) is shown in Fig. 6. As can be seen from the plot, the speed-up normally goes as the inverse of d/T and saturates at N, the number of phases available. Hence, the improvement achieved by this scheme is larger for small delays and smaller for large delays. Since the scheme based on DMU inherently provides resolution-bandwidth trade-off, the speed-up obtained can be used to reduce measurement time or increase accuracy over the single phase scheme.

There will be an error in the measurement if a certain phase does not span the delay completely. For instance, with an 8-phase clock, suppose the delay to be measured corresponds to one-fourth of the time-period, and the rising edge of 7th phase is chosen. Since, only 1/8th of the time-period is left, only half the delay will be counted, leading to an error in the measurement. Such cases can be avoided by having a conservative algorithm, wherein the delay count is updated

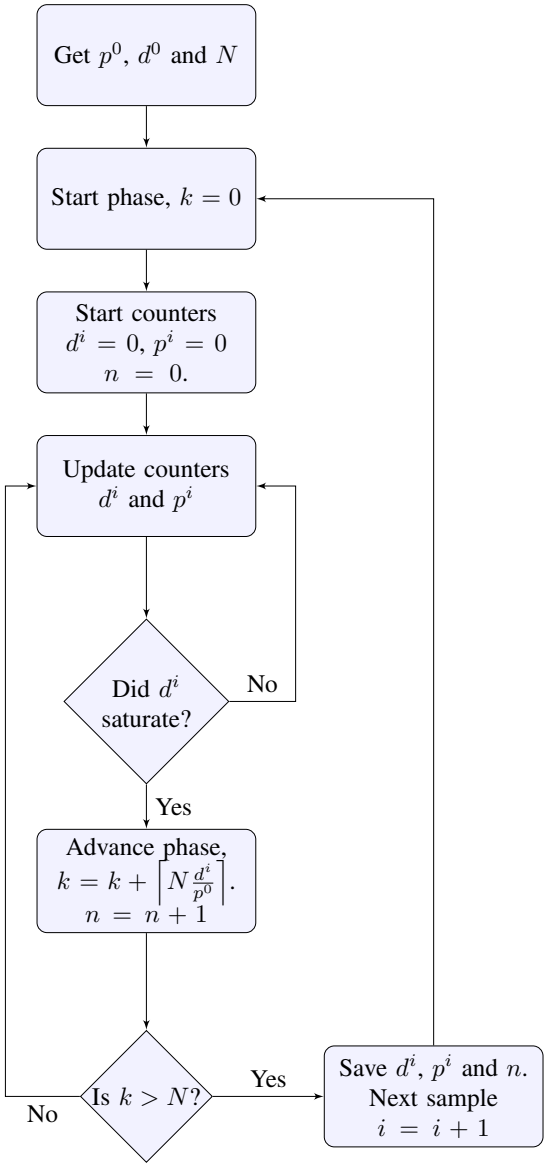

Fig. 7. Flowchart for the proposed scheme

N	Number of clock phases available
p^0	Period count in first beat period
d^0	Delay count in first beat period
p^i	Period count in i^{th} beat period
d^i	Delay count in i^{th} beat period
n	Number of clock phases used
k	Phase counter, ranges from 0 to $N-1$

if and only if it gets saturated which cannot happen unless a chosen phase fully covers the delay. If a certain phase fails to span the delay completely, the count corresponding to that phase is discarded. This approach also takes care of phase mismatch by being conservative, but might lose out slightly on speed-up.

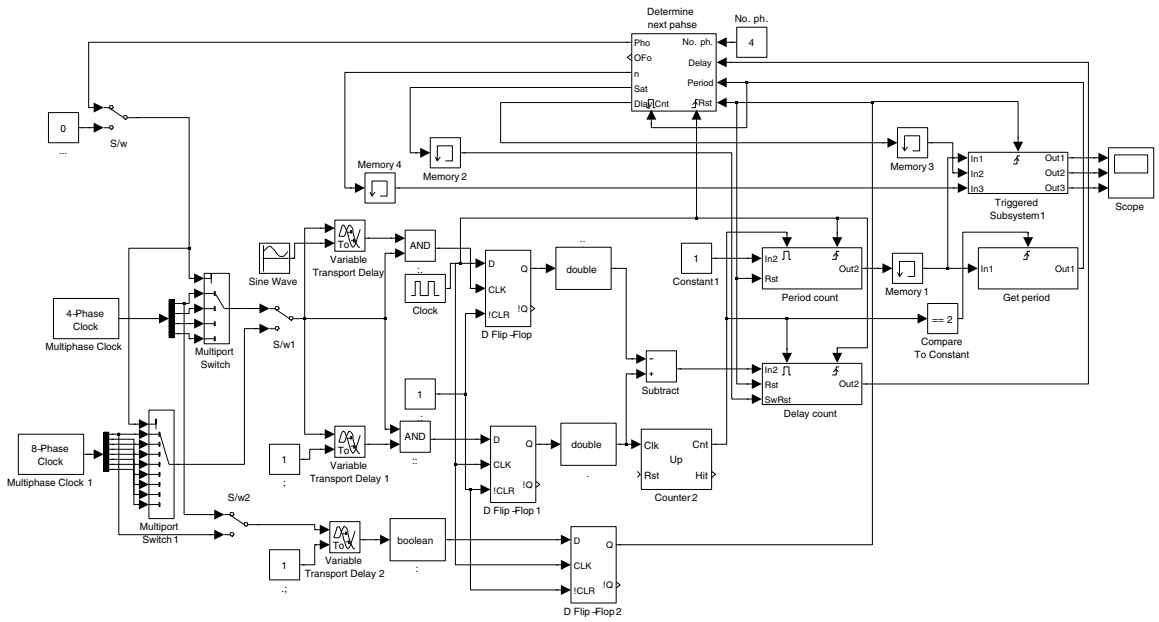

Fig. 8. Block diagram implemented in MATLAB Simulink

IV. Simulation

To verify the proposed idea, the system described above with the algorithm explained in flowchart Fig. 7 is implemented in MATLAB Simulink environment, the block diagram of which is shown in Fig. 8. An option is made to select one of single phase, 4-phase or 8-phase clock input to the DUT, which gives out a pair of clock signals between which a delay is setup. This clock pair is sampled by a sampling clock of slightly lesser frequency than the input clock. A pair of counters, one each for delay and period, are setup. The delay count is the accumulated arithmetic difference between the pair of sub-sampled outputs, while the period count is the accumulated number of rising edges of the sampling clock in a period of the sub-sampled output. The ratio of delay count to the period count is an unbiased estimate of the delay d as a fraction of the time-period T [9]. *Period count* and *Delay count* implement the appropriate counters, while *Determine phase shift* subsystem determines the phase-shift to be applied each time and generates control signals to reset the counters for every new measurement.

Simulation results for the case of fixed delay are tabulated in Table II for the parameters mentioned below the table. The point to be noted is that in entries 4, 5, 6 of Table II, the test delay of 0.5ns is much smaller than the basic quantization step of 4.72ns. Mean and standard deviation of 100 measurements are taken with the same setting. A larger standard deviation of the measured delay in the single phase case means that although the average of measured delays across measurements is quite close to the input delay, certain individual measurements may be off. Hence, the measurements with single phase clock will need more averaging to guarantee better accuracy, leading to increased measurement time. However, the standard deviation is lesser when multiphase input clock is employed, leading to reduced measurement time for a given accuracy.

In general, the variance of measured delay decreases inversely as the measurement time. Hence, if σ_1^2 and σ_N^2 be the variances of a certain measured delay, and T_1 and T_N be the respective measurement times, then

$$\frac{\sigma_1^2}{\sigma_N^2} = \frac{T_N}{T_1} \tag{5}$$

But, in this particular scheme, use of N-phase input clock yields a measurement of lesser variance. Hence, to achieve a given variance of the measured delay, the scheme with N-phase input clock takes lesser time. This speedup is roughly given by

$$\text{Speedup}, n = \frac{\sigma_1^2}{\sigma_N^2} \tag{6}$$

Entries of Table II confirm that speedup is more for small delays and is in close agreement with theoretically expected values.

It is shown in [16] that such delay measurement schemes can also handle slowly varying delays without the explicit use of sample-and-hold circuitry. However, the varying input, say a sine wave, should be suitably oversampled so that the test delay will not change by more than an LSB during the measurement time. If $d = A\sin(2\pi f_{in} t)$ is the test delay input and T_b is the measurement time, then

$$\begin{aligned} 2\pi A f_{in} T_b &\leq a \\ f_{in} &\leq \frac{a}{2\pi A T_b} \end{aligned} \tag{7}$$

where a is the LSB. With $T_b = 2.218\mu$s for 8 bits, f_{in} can

TABLE II
SUMMARY OF SIMULATION RESULTS FOR FIXED INPUT DELAY

Sl. No.	Input Delay (ns)	No. of phases	Measured Delay (ns) Mean	Std. deviation	Speedup over single phase
1		1	20.00	1.71	1
2	20	4	19.94	0.87	3.86
3		8	20.05	0.85	4.05
4		1	0.55	1.48	1
5	0.5	4	0.55	0.64	5.35
6		8	0.50	0.50	8.36

Setting:
Input clock frequency, $f_c = 10$ MHz
Sampling clock frequency, $f_s = 9.55$ MHz
Duration of beat period, $T_b = 2.218\mu$s
Basic quantization step, $\Delta T = 4.72$ ns
Jitter in both input and sampling clocks = 100ps.

TABLE III
SUMMARY OF SIMULATION RESULTS FOR SLOWLY VARYING DELAY

Sl. No.	Input Delay Amplitude (ns)	No. of phases	Measured Delay SNR (dB)
1		1	06.50
2	5	4	12.99
3		8	17.59
4		1	15.56
5	15	4	18.85
6		8	18.63

Setting:
Input sine frequency, $f_{in} = 484.15$ MHz
Oversampling ratio, OSR = 465.45

be atmost 560 Hz. Choosing[2] $fin = 484.15$Hz, we have the results for the different number of input clock phases summarized in Table III, with the other settings same as that of Table II. The SNR numbers reported here are before low pass filtering, and hence the SNR will improve after filtering and decimation. The results clearly show that SNR for small test delays improves in the case of multiple phases, although the increase may not be substantial for large test delays.

V. CONCLUSION

The method of time measurement using sub-sampling based DMU is briefly revisited and its limitation in measuring small delays is described. A solution to improve the speed (and/or accuracy) by making use of a multiphase input clock is described. Simulation results from MATLAB Simulink environment demonstrate a speed-up of upto a factor of eight achieved by an eight-phase input clock for fixed test delays and an improvement in SNR of upto 11dB for slowly varying test delays.

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[2]Chosen to ease computation of FFT by eliminating spectral leakage.

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