DESIGN OF FLIP-FLOPS WITH LOW SETUP AND HOLD TIMES ACROSS PROCESS VARIATIONS

Conference Paper · August 2007

CITATIONS
0

READS
19

3 authors, including:

Pratap Kumar Das
Achronix Semiconductors Corporation, Bangalore
8 PUBLICATIONS **32** CITATIONS

SEE PROFILE

DESIGN OF FLIP-FLOPS WITH LOW SETUP AND HOLD TIMES ACROSS PROCESS VARIATIONS

Pratap Kumar Das[1], Bharadwaj Amrutur[2], J. Sridhar[3]

Abstract

In this paper we investigate the impact of process fluctuations on the variability of the set-up and hold times of flip-flops. A set of flip-flops available in the literature are discussed in the context of low uncertainty window for sampler type of applications. We find that differential sense amplifier flops show less variability than single ended ones, due to the inherent properties of the differential structure. We suggest a simple technique to generate a built in reference for a differential flop, which enables its application in single ended digital type applications, but still preserves all the robustness properties of a fully differential structure. We have evaluated the flops in an industrial 65nm process and simulation results show that our proposed flop has around 5X reduction in its uncertainty window compared to a single ended standard master slave flop, as well as about 2X reduction in the variations in the window across process corners. Our proposed structure also maintains almost constant uncertainty window over the supply voltages from 1.1V to 0.8V unlike the single ended flops.

Keywords: Samplers, Variability, Sense Amplifier, Flip-flop.

1. Introduction

Samplers [1] or flip-flops are integral elements of any digital system and with technology scaling down and increasing clock speed, the non idealities of the flip-flops are becoming more important. Some of the important design parameters of the flip-flop are the setup time, hold time, power and the clock to output delay [1] which affect the latency and the speed of the over all system. But when the samplers are used to capture data which is asynchronous to the sampling clock, the timing parameter of interest is the sum of the setup and hold times i.e. the total uncertainty window given as $\tau_{setup\text{-}hold} = \tau_{setup} + \tau_{hold}$ [1]. In such applications, not only should the uncertainty window be small, its variations due to process fluctuations across a chip should also be minimized. With scaling into deep submicron technologies, the process parameter variations are expected to increase and hence one can expect larger variations in circuit operation. In this work we study the impact of process fluctuations on the

1. Department of ECE, IISc, Bangalore, India, Email: pratap@ece.iisc.ernet.in
2. Department of ECE, IISc, Bangalore, India, Email: amrutur@ece.iisc.ernet.in
3. TI, Bangalore, India, Email: jsridhar@ti.com

variations in the uncertainty window of the samplers and look for ways to mitigate it.

There are various kinds of flip-flops described in the literature. These include, single ended ones such as the standard Master-Slave flip-flop, Dynamic Transmission Gate edge triggered Register, C^2MOS, and Truly Single Phase Clocked Register [2] and differential ones such as Sense-amplifier-based Poulton-Dally-Tell Sampler (PDT Sampler) [3], Semi-dynamic single ended/double ended flip-flop (SDFF) [4], Differential skew tolerant flip-flops [5] and Sense-amplifier based flip-flops proposed by Nicolic et al. [6] ,Kim et al.[7], Antonio et al. [8]. The works in [6-8] focus on reducing the clock to output delay and don't address the variations in the flop's uncertainty window.

Each type of flip-flop is optimized to improve some particular aspect of the sampling and storage action. For the problem we are considering, namely minimization of the variation of the sampler's uncertainty window, we can consider the behavior of single ended flops versus the differential flops. All single ended flops compare the input data signal with an implicit reference within the flop which can eventually be traced to the trip point of some inverter type structure. Hence these flops are very susceptible to process variations, especially when there is relative skew between the PMOS and NMOS transistors. On the other hand, differential flops compare the signal to its complement and hence we can expect them to be more tolerant to process variations. Since most digital applications have single ended signals, we need to provide an appropriate signal for the complementary input of a differential flop. We suggest a simple technique to generate a reference and we discuss this further in Section 2. Section 3 shows the comparison results for the various flops. In order to perform a fair comparison all the flip-flops are optimized to have minimum uncertainty window under typical operating conditions. We present our conclusions in Section 4.

2. Analysis of flip-flops from variability perspective

Let's first consider the standard Master-Slave D flip-flop (MSDFF) in Fig. 1 which is given as a representative for all single ended flops.

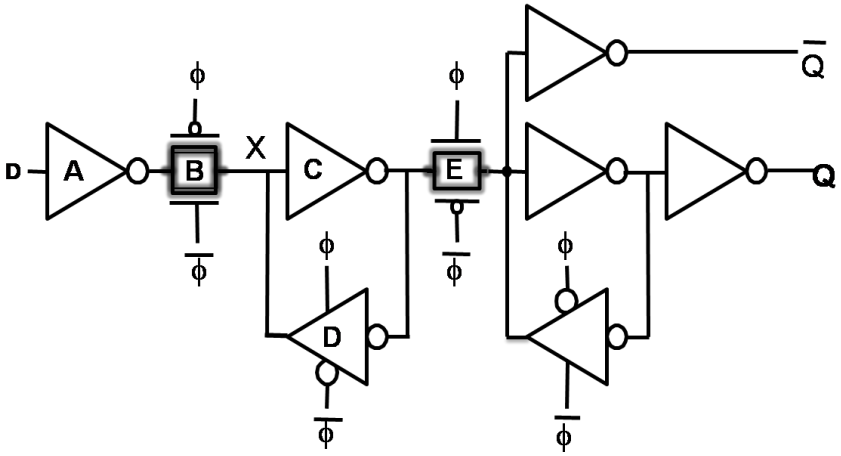

Figure 1: Master Slave Flip-flop

In this flip-flop the data is sampled by the clock on the rising edge wherein the master latch transitions from the transparent to the opaque state. The setup and hold window is determined by the propagation delays through the gates labeled A, B and the cross coupled gates C & D as the clock transitions from one logic level to the other. Process fluctuations will cause variations in the delays of these gates as well as the characteristics of the cross coupled gates C & D and hence cause variations in the setup-hold window. We can also observe that the gates C & D are not identical and hence the characteristics of the cross coupled structure C & D will be sensitive to local mismatches in the transistors. Hence all single ended schemes [2] will tend to be more susceptible to process variability.

Let's now consider the case of differential flip-flops. In fact there are several types of flip-flops available in the literature as mentioned above. But all the sense amplifier flops have a common template, which consists of a cross coupled inverter pair, which starts in a high impedance state. The input differential signal is transferred onto the nodes of the inverter pair and the sampling clock edge initiates the regenerative action. An example differential flop is shown in the Fig. 2 ([3, 11]). This flop is extensively used in various samplers due to some of its interesting properties such as near-zero setup time, a reduced hold time, a low clock load and true single phase operation.

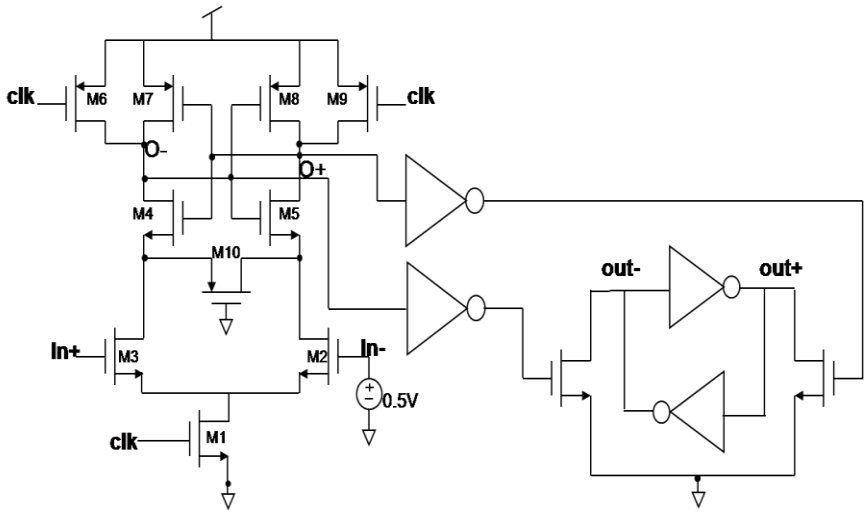

Fig. 2: Poulton-Dally-Tell Sampler [11]

For a single ended application, the In- input can be connected to a fixed voltage reference as shown in the figure.

The operation of the above circuit is as follows. When clk is low, the nodes O+ and O- are precharged to high and the slave stage consisting of back-to-back inverters holds on to the values stored in the previous stage at out+ and out-. At the rising edge of the clock, the bottom transistor M1 is turned on and hence there is a current flow through the stack of transistors. The differential voltage between In+ and In- is transferred as a differential current between the two pull

down legs. This creates a small differential voltage between O+ and O- which eventually gets regenerated into full digital levels by the cross coupled pair of inverters M4,M7 and M5,M8. The setup-hold window here is governed by the transfer time across the input transconductance pair M2-3 as well as M4-5, the regeneration time constant of the cross coupled latch M4,M7,M5,M8 as well as the clock rise time [12]. Because the number of devices in the path from input signal to capture is small (only M2 and M4), we can expect a smaller setup-hold window as well as a smaller variation in the same. Moreover, the differential nature allows a symmetric design for each half of the flop, allowing for reduced impact of local mismatches. As another data point for differential flops, we consider a recently proposed modification to the PDT flop [8], reproduced in Fig. 3.

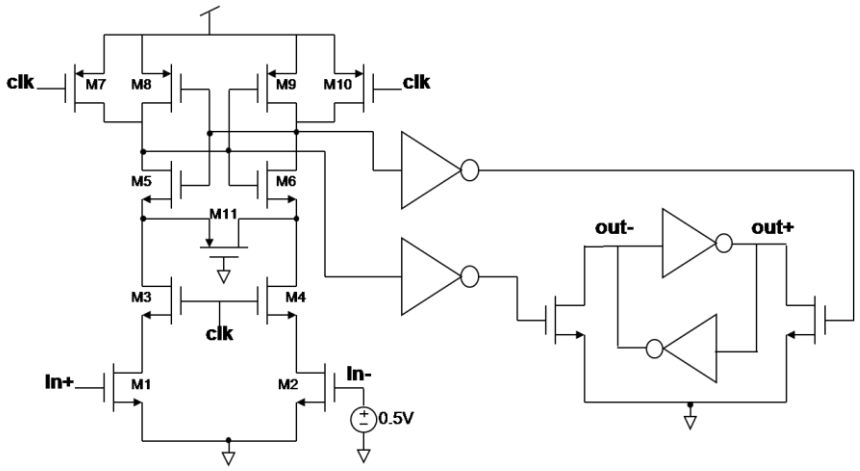

Fig. 3: Modified Poulton-Dally-Tell Sampler [8]

The main change in this circuit is that the Clock signal transistors are moved up above the input transistors. With this change there is a higher over drive voltage for the Input transistors than the previous circuit as well as a reduction in the body effect. This enables a faster operation as well as reduced offsets. Similar to the case of the PDT flops, we would expect a variability of the setup - hold times to process fluctuations.

Generation and distribution of a reference voltage is troublesome in digital applications. Instead, we suggest a simple method to generate a built-in reference as shown in Figures 4 & 5. The input transistors M2 & 3 of the original samplers are split into two segments M2a,b and M3a,b. In+ is fed to both M3a&b transistors, while the gates of M3a&b are tied to supply and ground respectively. The idea is to create a reference current in complementary leg, which is somewhere in between the currents of the signal leg, for input of Vdd and input of Gnd. A similar technique is widely used for introducing offsets in samplers.

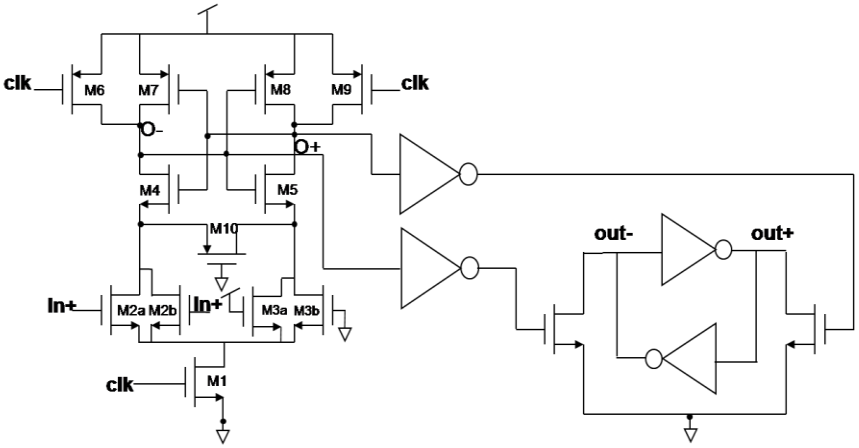

Fig. 4: Self Referenced Poulton-Dally-Tell Sampler (SRPDT)

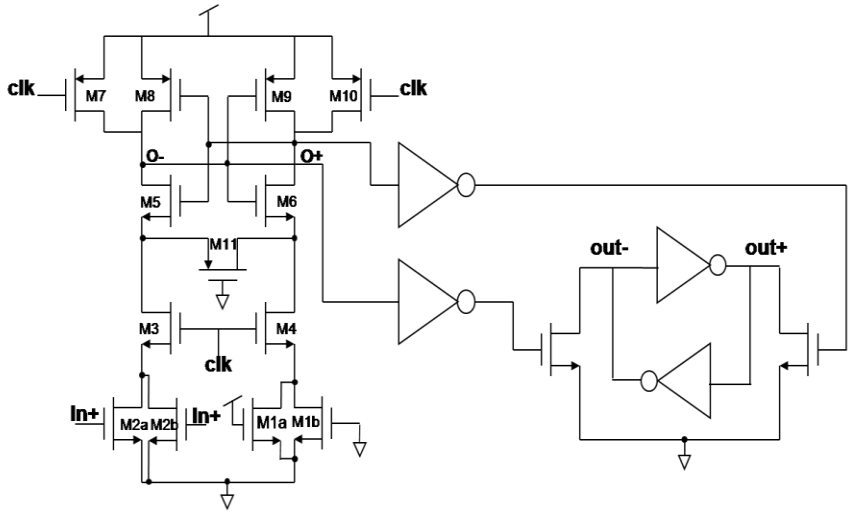

Fig. 5: Self Referenced Modified Poulton-Dally-Tell sampler(SRMPDT)

.

3. Simulation Results and Comparison

We use the method proposed in **[10]** for measurement of the setup and hold windows, which measures the data to clock delay for which the clock to Q delay will be minimum.

Figure 6 shows the variation of the uncertainty window across corners for different flip-flops. The MSDFF and PDT flops are designed to minimize their respective uncertainty windows **[10].**

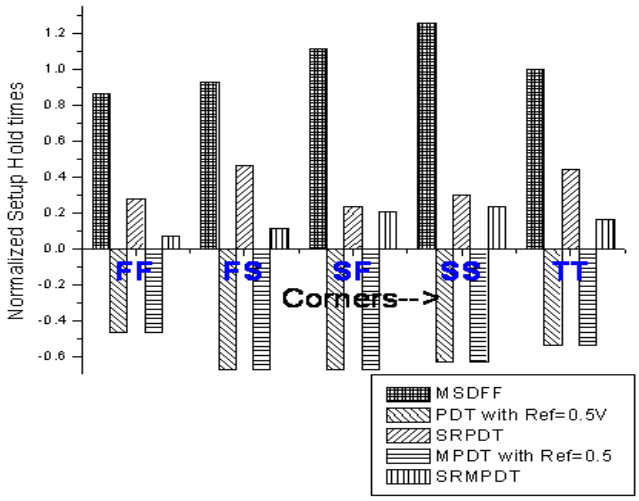

Fig. 6 : Normalized Uncertainty windows across various corners for different flops .

All the data shown in this paper are normalized to the setup-hold window of the MSDFF under typical process corners. Fast, Slow and Typical transistors are labeled as F, S & T respectively, with the first label referring to the NMOS and the second to PMOS. All the differential flops have a smaller setup-hold window, as well as smaller variations in the window across process corners. For instance the SRMPDT's uncertainty window is only 0.2X of that of the MSDFF in the TT corner and the variations in the window across process corners is reduced by half. The smaller setup-hold window can be attributed to the shorter path between input to the decision latch. The smaller variations can be attributed to the differential nature.

Table 1 summarizes all the results and show that the differential samplers have about two times lower variation than the standard Master Slave D Flip-flop.

Table-1 Max and Min Variation of Set-up-hold window for different flops:

Type of F/F →	**PDT**	**SRPDT**	**MPDT**	**SRMPDT**	**MS DFF**
Max Setup/Hold	-0.68	0.46	-0.67	0.23	1.25
Min Setup/Hold	-0.46	0.24	-0.46	0.06	0.86
Variation	0.22	0.22	0.21	0.17	0.39

Note that the positive values indicate setup time problems and negative value indicates hold time problems for the flops. We can also observe that the MPDT and SRMPDT's uncertainty window is less compared to PDT and SRPDT. This can be attributed to the lower setup-hold time for these flops as illustrated in Figure 6. Figure 7 shows the normalized delay from the rising edge of the Clock

to Sense amplifier output stage for the four different types of sense amplifier flops. The decrease in the Clock to Sense amplifier delays while using the modified PDT structure is apparent from the figure.

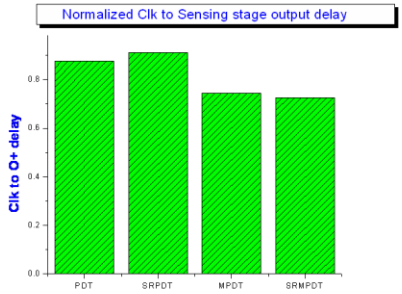

Fig. 7 : Normalized Clock to Sensing stage Output delay.

Figure 8 shows the average power consumed for each type of flop under similar conditions. Power is measured with the data to Clock delay being fixed to a constant value. The input data transition is chosen such that within a period of power evaluation, there is transition of each type (i.e. 0 →0, 0→1, 1→0, 1→1) at the output. With this condition imposed on all the five type of flops the power numbers show the following trend for various flops. The DFF has the least power as it can take advantage of data activity factor, where as the sense amplifier flops are precharged in each cycle independent of the data activity. The MPDT and SRMPDT flops show about 44% reduction in power compared to PDT and SRPDT. This is because of the lower regeneration times in these flops as shown in Figure 7. The power dissipation of these flops is the largest during regeneration and hence faster regeneration reduces power.

Figure 9 shows the normalized uncertainty window across supply voltages from 0.8V to 1.1V. The variation in uncertainty window is shown as an error bar for each voltage point. We can observe that the variations in the uncertainty windows for the differential flops, PDT and SRMPDT, remain almost constant across the supply voltage range, whereas for the MSDFF the variations increase with reduced supply. We can also observe that the mean uncertainty window doesn't change much for the differential flops as compared to the single ended one across supplies. This can again be attributed to the more robust differential structure. There is a slight variation in the mean uncertainty window for the PDT as compared to the SRMPDT since the former uses a fixed external reference, while the latter uses a built-in reference. Hence we can conclude that the differential flops in general and the Self-referenced flops in particular are very robust against the process as well as the supply voltage variations.

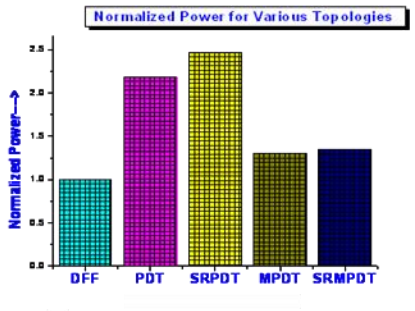

Fig. 8 Normalized average Power across Various Types of flops.

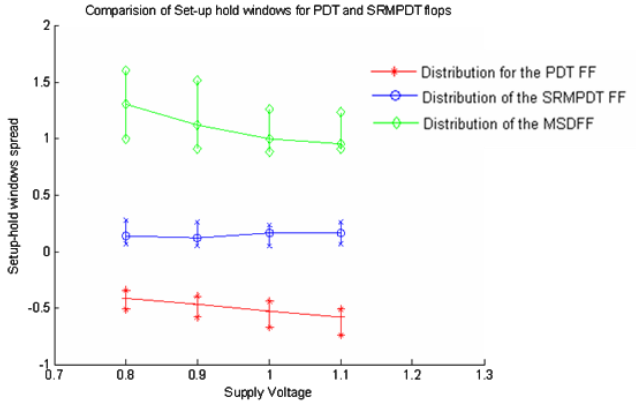

Fig. 9 Normalized Uncertainty window across supply voltage

4. Conclusions

We have studied the effect of process fluctuations on the uncertainty windows of edge triggered flops. As expected, the differential flops show more robustness to process and supply voltage variations, compared to the single ended flops. We have suggested a simple scheme to generate a built-in reference for the differential flops. This enables a compact, self-contained structure, which still has all the robustness properties of differential structures. In comparison with a single ended master slave flop, we find that the proposed SRMPDT flop has a 5x reduction in the uncertainty window as well as a 2x reduction in the variation of the window across process corners. It also maintains almost constant window from 1.1V to 0.8V unlike the single ended flop. While it consumes about 25% more power than a single ended flop, it consumes about 44% less power as compared to the conventional differential flop.

References

[1] Fei Yuan "*CMOS Current-Mode Circuits for Data Communications*" Springer Publication,2007

[2] John M. Rabaey, "*Digital Integrated Circuits : A Design Perspective*". Second Edition, Prentice-Hall Publication.2002.
[3] M. Matsui, H. Hara, Y. Uetani, L. Kim, T. Nagamatsu, Y. Watanabe, A. Chiba, K. Matsuda, and T. Sakurai, "*A 200 MHz 13 mm^2 2-D DCT gMacrocell Using Sense-Amplifying Pipeline Flip-Flop Scheme*". IEEE J.Solid-state Circuits, vol. 29, no. 12, pp. 1482–1490, Dec. 1994.
[4] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R.Wang, A. Mehta, R. Heald, and G. Yee, "*A new family of semidynamic and dynamic flipflops with embedded logic for high-performance processors,*" IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 712–716, May 1999.
[5] H. Partovi, R. Burd, U. Salim, F. Weber, L. D. Gregorio, and D. Draper, "*Flow-through latch and edge-triggered flip-flop hybrid elements*," in Proc. Int. Solid-State Circuits Conf., 1996, pp. 138–139.
[6] B. Nikolic, V. G. Oklobdzija, V. Stajanovic, W. Jia, J. K. Chiu, and M.M. Leung, "*Improved sense-amplifier based flip-flop: Design and measurements,*" IEEE J. Solid-State Circuits, vol. 35, no. 6, pp. 876–883, Jun. 2000.
[7] J. Kim, Y. Jang, and H. Park, "*CMOS sense-amplifier based flip-flop with two N-C MOS output latches,*" Electron. Lett., vol. 36, no. 6, pp. 498–500, Mar. 2000.
[8] Antonio G. M. Strollo, Davide De Caro, Ettore Napoli, and Nicola Petra, "*A Novel High-Speed Sense-Amplifier-Based Flip-Flop*" IEEE Transactions On VLSI Systems, Vol. 13, pp. 1266-1274, Nov. 2005.
[9] Vijay U.K., Bharadwaj Amrutur, "*Continuous Time Sigma Delta Modulator Employing a Novel Comparator Architecture*". 20th International conference on VLSI Design, January 2007.
[10] V. Stojanovic and V. G. Oklobdzija, "*Comparative analysis of master-slave latches and flip-flops for high-performance and low-power systems"*. IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.
[11] W. Dally and F. Yuan. "*Transmitter equalization for 4-Gbps Signalling,*" IEEE Micro, 17(1):48-56,Jan/Feb. 1997.
[12] R. Sarpeshkar, et. al., "*Mismatch sensitivity of a simultaneously latched CMOS Sense amplifier*", IEEE J. of Solid-State Circuits, vol. 26, pp. 1413-1422, Oct. 1991.