SRAM: Timing Generation

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Timing

CLK

WLN

PDE

Y_rq

CAE
Timing Generation

Diagram showing a circuit with labels such as Row, Decoder, NLE, Timing Generation Block, WL, PRE, SAE, and PRE Charge. The diagram includes signals and connections like Address, Read/Write, Clock (CLK), and timing generation related components.
SRAM Timing Parameters
Inside Tcycle
Basic Timing Generation

Pulse timing controlled by clock duty cycle: + robust - energy - speed
Timing requirements

CLK

WL

b, ̅b

SAC

twor-width

ΔV_{min} \geq \Delta V_{sa-offset}

\text{tsae-oh} \geq 0
Sense amp offset

Mismatch:
1. Line edge roughness \( \Delta L, \Delta W \)
2. Gate layout orientation
3. Current direction

\( \Delta V \) \text{min} \geq 5 \text{mV}

Increasing \( W, L \) reduces mismatch (random)
Replica Based Self-Timing

[Amrutur, JSSC, Aug 1998]
Replica timing relationships
Delay matching of two paths

Match sum of falling in each chain, and sum of rising in each chain (NMOS pulldowns match each other, PMOS pullups match each other)
Replica cell layout
Enhancements

• Only one replica cell to mimic the entire array
  – Doesn’t work well with increased random cell to cell variations

• Use multiple replica cells to pull down replica bitline
  – Better estimate of the array’s average cell current