0.5V SUBTHRESHOLD REGION OPERATED ULTRA LOW POWER PASSIVE SIGMA DELTA ADC IN 180NM CMOS TECHNOLOGY

by
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I certify that I have read this thesis and that, in my opinion, it is fully adequate in scope and quality as a thesis for the degree of Master Of Science (Engineering).

______________________________
(Dr Bharadwaj Amrutur) Principal Advisor
To
Everyone who dreams
and
The Majesty
ACKNOWLEDGMENTS

This study would not have been possible without the support of several people who have contributed in my journey immeasurably. I take this opportunity to offer my sincere gratitude to each of them.

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Abstract

With increasing demand of IoT devices, medical devices, remote sensors; the design of low power analog interface is becoming focus. Generally, for low frequency applications the Sigma Delta ADCs are used due to their very good resolution capability for such interfaces. Hence extensive work is being done to design ultra-low power Sigma Delta ADC. Most of the work has been done on optimizing loop filter design both in terms of architecture and its basic building element, op-amps. Recently, one of the prime focus of such research is Passive Sigma Delta ADC, where the loop filter is implemented with passive elements instead of active elements like op-amp.

In this work, a subthreshold region operated Passive Sigma Delta design has been explored. The thesis discusses a different analytical approach to analyze passive SDM ADC than the usual circuit level analysis used traditionally. The Simulink modeling of a passive SDM ADC was addressed to study block level performance. The circuit level implementation was carried out in Cadence environment. Both pre-and-post layout level simulations were conducted.

The passive SDM ADC designed in this work has a Sampling frequency of 10MHz, with a signal BW of 10KHz. An ENOB of 10.4 bits is achieved at power dissipation of only 4µW. The proposed ADC has very competitive FOM (Figure of Merit) in comparison with published literature.
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### NOTATIONS/ABBREVIATIONS

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<th>Abbreviation</th>
<th>Full Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>SDM</td>
<td>Sigma Delta Modulator</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>PSC</td>
<td>Passive Switch Capacitor</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number Of Bits</td>
</tr>
<tr>
<td>FoM</td>
<td>Figure of Merit</td>
</tr>
<tr>
<td>STF</td>
<td>Signal Transfer Function</td>
</tr>
<tr>
<td>NTF</td>
<td>Noise Transfer Function</td>
</tr>
<tr>
<td>DTF</td>
<td>Distortion Transfer Function</td>
</tr>
</tbody>
</table>
Recently there has been an increasing demand of remote sensors in fields like medical and health care [1-5], wearables [6-7] and MEMS based sensors [8-10] for temperature, pressure, etc. measurements. Often most of these systems are low frequency applications and are driven by either batteries or harvested energy. In applications like IoT once such sensors are deployed in the field, the whole idea is to have long operational life of these sensor nodes. Hence the design goals have shifted to medium resolution-low frequency with ultra-low power dissipation from very high-resolution systems. Also in general, redundancy is introduced in such systems which facilitates the improvement of overall accuracy/reliability of the system but imposes higher energy costs; hence it becomes even more essential to reduce the power consumption of every node.

A typical sensor system includes a front-end amplifier and filter circuit followed by an Analog to Digital Converter (ADC). The digitized output is then passed over to either microprocessor/microcontroller (as shown in fig.1) or transmitted through an antenna depending on the application. The ADC is one of the most crucial element of the sensor interface and needs special attention.

In this work the sensor considered is a MEMS based pressure sensor with differential output. The objective of the work here is to design an ultra-low power ADC for these sensor interfaces.
Sigma Delta Modulator (SDM) based ADCs are most suitable for low frequency-high resolution applications. In this work, various methods to limit the power of SDM have been discussed and a passive integrator based SDM has been designed and implemented.

1.1 Thesis guide

The thesis is divided into 6 chapters. In chapter 2 basics of continuous SDM ADC in terms of noise shaping is described. It also lists the advantages and dis-advantages of both continuous and discrete time SDM which in-turn helps to determine the suitable architecture for this work. The important parameters associated with SDM ADC performance have been discussed in this chapter.

Chapter 3 includes discussion on various methods to reduce power consumption of SDM ADC. It also discusses the previous work done in passive SDM design and helps to build the understanding through the literature.

In chapter 4, a system level quantitative analysis of considered Passive SDM (PSDM) architecture is carried out, a different approach than the reference is taken up in this work. Thereafter, the design is simulated in MATLAB Simulink using inbuilt ideal components to study the architecture and learn the impact of various components on the performance of PSDM.
Chapter 5 focusses on the circuit level implementation of ADC in Cadence environment, a comparison of performance in various process corners has been studied and finally chapter 6 includes the performance results.
Chapter 2
Basics of Sigma Delta Modulator ADC

Analog to digital conversion is the heart of any data processing system. The conversion is carried out in two steps: Sampling the continuous physical signal (time domain discretization) and then Quantizing the sampled value (amplitude discretization).

Depending on the sampling rate these ADCs are classified as:

a. Nyquist rate based ADC: here the sampling rate is twice of the BW of the signal to faithfully reconstruct the signal.
   Example: Successive Approximation Register (SAR), Flash ADC, Pipeline ADC, Dual Slope Integrating ADC.

b. Oversampling based ADC: In such ADCs the signal is sampled at much higher rate than the Nyquist criteria. Later, a digital decimation filter is used to scale down the sample rate to 2*BW.
   The oversampling is expressed in terms of Over-Sampling Ratio (OSR) which is equal to ratio of sampling frequency (Fs) to the Nyquist rate (2*BW).
   Example: Sigma Delta ADC

The Nyquist rate ADCs are memoryless and there exists one-to-one mapping of input and output samples. However, in case of oversampling ADCs, the conversion is memory-assisted and one output sample of ADC depends on multiple input samples (equal to OSR). Table 2.1 summarizes the performance of these ADCs.
Table 1: ADC architectures and their comparison

<table>
<thead>
<tr>
<th>Architectures</th>
<th>Speed</th>
<th>Resolution</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Integrating</td>
<td>Low</td>
<td>High</td>
<td>Instrumentation &amp; Measurement</td>
</tr>
<tr>
<td>SAR</td>
<td>Low-Medium</td>
<td>Medium</td>
<td>Biomedical, Control</td>
</tr>
<tr>
<td>Flash</td>
<td>High</td>
<td>Low-Medium</td>
<td>RF &amp; Microwave, Video</td>
</tr>
<tr>
<td>Pipelined</td>
<td>High</td>
<td>Medium</td>
<td>RF &amp; Microwave, Video</td>
</tr>
<tr>
<td>Sigma-Delta</td>
<td>Low-Medium</td>
<td>Medium-High</td>
<td>Audio, Biomedical</td>
</tr>
</tbody>
</table>

2.1 Sigma Delta ADC basics and principle

For every ADC, the process of sampling and quantizing i.e. converting continuous waveform into digital discrete waveform, results in addition of quantization noise. The true digital representation of the signal depends on this quantization error which should be within ±0.5LSB (Least Significant Bit). The reduction in quantization error in Sigma Delta ADC is mainly achieved by oversampling (averaging the multiple samples) and noise shaping the in-band (within signal BW) quantization white noise by high pass characteristic (explained in detail, later). In this way, the total noise present within in-band is reduced significantly; resulting in very high resolution. Based on this property of SDM, there have been SDM with performance as good as 24-bit resolution or more [11-12]. Fig.2 shows how SDM ADC shapes the in-band noise (the figure is not to scale and just depicts the phenomenon of noise shaping).

![Figure 2: Quantization Noise in Sigma Delta ADC](image)
The generic block diagram of sigma-delta ADC is as shown in the figure below. The SDM architecture is a mixed-signal design, and includes both analog and digital blocks as explained subsequently.

![Figure 3: Generic block diagram of Sigma Delta ADC](image)

<table>
<thead>
<tr>
<th>Analog Input</th>
<th>Anti-aliasing Filter</th>
<th>Modulator</th>
<th>Decimation Filter</th>
<th>Digital Output</th>
</tr>
</thead>
</table>

![Figure 4: Sigma Delta Modulator](image)

<table>
<thead>
<tr>
<th>Analog Signal</th>
<th>Sample-n-Hold</th>
<th>Loop Filter</th>
<th>Quantizer</th>
<th>Digital Output</th>
</tr>
</thead>
</table>

**a. Anti-aliasing Filter:** It is a band limiting filter which attenuates high frequency signals (out of band). From Fourier analysis of sampled signal [13], we can observe that in frequency domain; the signal is periodic with periodicity of $F_s$ Hz. Since in case of oversampled ADCs, $F_s$ is very large compared to $f_{in}$, the design requirements for anti-aliasing filter is relaxed and a lower order filter can suffice the purpose. Also since the order of filter is lower, the power consumed by Anti-aliasing filter is brought down significantly.

**b. Modulator:** It is the heart of sigma delta ADC. The modulator consists of a sample and hold circuit, which operates at $F_s (>>2*f_{in})$. The sampled data is then quantized
using sigma delta integrator based modulator (derived from delta modulator, read [14] for history of sigma-delta ADC)

c. Decimation Filter: The main purpose of decimation filter is to suppress the high frequency noise component and to downscale the output rate from oversampled rate to Nyquist rate.

The crucial part of sigma delta ADC design is the sigma-delta modulator. The performance of ADC is actually the measure of how well the modulator is implemented. The modulator can be either discrete time or continuous time based. The detailed study of them can be referred in [15]. Here, only comparison between both CT and DT SDMs have been drawn to determine the suitable architecture for this work (in later part of this chapter).

The block diagram of sigma delta modulator is as shown in figure 4. It mainly consists of sample-n-hold (sometimes excluded from main modulator design), the loop filter, quantizer and feedback network using DAC. Both quantizer and DAC modules are clocked at sampling frequency.

a. Sample-n-Hold circuit: This module is essential in discrete modulator design whereas in continuous time sigma delta modulator it can be eliminated and the sampling is performed as a part of modulator by clocking the quantizer. Generally, these circuits are build using op-amps and hence consume lot of power. Also, another design constraint is to design switches, especially in low voltage applications.

b. Loop Filter: The noise shaping performance of sigma delta modulator is mainly governed by the order of the Loop Filter. It determines the number of zeros present in Noise Transfer Function (NTF) and hence the high pass characteristic of modulator for quantizer’s noise. One of the advantages of CT SDM is it provides low pass characteristic to signal input and hence the design of an anti-aliasing filter
can either be relaxed or eliminated completely. The order of modulator also
determines the roll-off rate for this signal low pass characteristic. As the order of
loop filter increases, the desired performance can be achieved at lower OSR value.
The noise shaping performance of various order loop filter can be studied in [15-
17]

Loop filters are essentially integrators (in case of low pass modulators) and are built
using switched capacitor and RC based op-amp integrators in DT and CT SDM
respectively.

c. Quantizer: This block is the primary source of non-linearity present in the sigma
delta ADC. The quantization noise added by this module is filtered by the loop
filter. The quantizer is usually implemented with high-speed-high-input-dynamic
range (swing-to-swing preferably) performance and is clock operated. Due to
averaging, the design requirements of quantizer are bit relaxed, nevertheless it is
still essential in determining the performance of ADC. Further, the quantizer can
be either single bit or multi bit. The noise shaping performance and linearity is
improved with multi bit quantizer. However, the design of both modulator and
decimation filter becomes complex [18-20].

d. DAC: DAC provides the feedback by converting digital output into analog signal
w.r.t. some reference. The DAC can operate in either voltage or current mode.
There are three major shapes of DAC pulses, Non-Return-to-Zero (NRZ), Return-
to-Zero (RZ) and Half-Return-to-Zero (HRZ); each has its own advantages
specially in terms of jitter immunity and has been studied in [21-25]. A few of the
challenges involved in design of DAC are: to implement linear DAC circuit in case
of multi-bit SDM, and any excess delay [26-28] that can cause memory effect from
previous clock. Both these have been extensively studied in terms of stability and
overall performance. On the other hand, single bit quantizer relaxes the design of
DAC and enable the use of a simple inverter based structure.
### 2.2 Continuous Time v/s Discrete Time SDM:

In this section, a comparison is drawn between CT and DT SDMs to decide upon the architecture to be used in this work. A detailed study of both the architectures can be found in reference [15].

<table>
<thead>
<tr>
<th>Advantages</th>
<th>CT-SDM</th>
<th>DT-SDM</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Built-in anti-aliasing filter</td>
<td>Analysis and modeling is easier</td>
</tr>
<tr>
<td></td>
<td>Slew rate and Unity Gain Bandwidth (UGB)</td>
<td>Capacitor ratio decides loop filter performance and hence better accuracy achievable</td>
</tr>
<tr>
<td></td>
<td>specifications are not stringent</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Jitter noise (present at the sampler)</td>
<td>Less susceptible to process variation, as integrator gain is determined by capacitor ratios, so lesser impact of process variation</td>
</tr>
<tr>
<td></td>
<td>experiences same transfer function</td>
<td></td>
</tr>
<tr>
<td></td>
<td>quantization noise</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Suitable for high sampling frequency</td>
<td>Scaling with clock frequency</td>
</tr>
<tr>
<td>Disadvantage</td>
<td>Pole location is not scaled with frequency, hence suitable for only one clock frequency</td>
<td>Switch non-linearity, charge injection, etc. causes error</td>
</tr>
<tr>
<td></td>
<td>Needs large capacitor (to limit thermal noise, lower R)</td>
<td>Sampling frequency &lt;f_t/100, where f_t is UGW</td>
</tr>
<tr>
<td></td>
<td>Sensitive to feedback pulse and duration</td>
<td>Required anti-aliasing filter</td>
</tr>
<tr>
<td></td>
<td>CMRR performance is poor due to any mismatch in resistors</td>
<td>Switch capacitor implementation introduces inherent glitches.</td>
</tr>
</tbody>
</table>

From the above comparison, it can be observed that for low power applications, continuous time SDM is more suitable than discrete time SDM.

### 2.3 Important parameters:

Generally, Nyquist based ADCs are characterized in terms of DNL and INL, however for oversampling ADCs; following parameters are important to characterize [29]:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
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</table>
1. **Signal-to-Noise ratio (SNR)**

The SNR characterizes the ratio of the fundamental signal power to the total noise spectrum power. The noise spectrum includes all non-fundamental spectral components present within the desired frequency range (in case of Nyquist rate ADC it is equal to sampling frequency / 2 however in case of oversampling frequency it is equal to sampling frequency / (2*OSR)) and the DC component & all harmonics present within the desired BW are neglected.

\[
SNR = 20 \cdot \log_{10} \left[ \frac{\text{Fundamental signal amplitude}}{\sqrt{\text{SUM} \left( \sqrt{\text{SQR(each Noise bin amplitude)}} \right)}} \right]
\]

2. **Spurious Free Dynamic Range (SFDR)**

The SFDR (or dynamic range) characterizes the ratio between the fundamental signal power and the highest spurious in the spectrum.

\[
SFDR = 20 \cdot \log_{10} \left[ \frac{\text{Fundamental signal amplitude}}{\text{Highest Spurious amplitude}} \right]
\]

3. **Signal-to-(Noise+Distortion) ratio (SINAD or SNDR)**

Here apart from noise bins, harmonic bins power is also included in measurement.

\[
SNDR = 20 \cdot \log_{10} \left[ \frac{\text{Fundamental signal amplitude}}{\sqrt{\text{SUM} \left( \sqrt{\text{SQR(each Noise bin amplitude + Harmonic bin amplitude)}} \right)}} \right]
\]

4. **Effective Number of Bits (ENOB)**

This is a measure of how effective the ADC is in terms of number of bits resolution.

\[
ENOB = \frac{(SNDR - 1.76)}{6.02}
\]
The following figure helps to understand the above-mentioned parameters.

![Figure 5: SDM ADC parameters definition](image)

5. Figure of Merit (FoM)

Apart from above mentioned parameters, the SDM ADC is also characterized in terms of FoM given by:

\[
FoM = \frac{P_d}{(2 \times BW \times 2^{ENOB})}
\]

where, \(P_d\) is power dissipated, \(BW\) is BW of ADC and \(ENOB\) is as defined above.
Chapter 3

Power reduction techniques in CT-SDM ADC

The idea of reducing power consumed by SDM has been the focus of analog front-end design, especially in sub-nanometer technology. In the previous chapter, it was concluded that continuous SDM is more suitable since power hungry sample-n-hold and anti-aliasing circuits are not needed unlike in DT-SDM. A few solutions have been suggested in literature on both architectural and circuit level optimizations for ultra-low power designs. This chapter discusses the prior work performed in this category. Further, to reduce the power consumption, design engineers are extensively utilizing the subthreshold region performance of MOS. The details of subthreshold region and challenges involved in design are also addressed in this chapter.

3.1 Subthreshold region operation and design:

Lately both analog and digital engineers are focusing on subthreshold region ($V_{gs} < V_{th}$) circuit design. In subthreshold region the inversion charge is very less than the source to drain region which leads to very low device current in this region [30], therefore for low power designs subthreshold region becomes focus of interest. However, as the device current has exponential dependence on $V_{gs}$, any small variation in bias voltage results in large fluctuation in current.

\[ I_d = K \cdot \exp \left( \frac{V_{gs} - V_{th}}{n \cdot V_T} \right) \]

In above equation, $V_{th}$ is the threshold voltage of MOS and $V_T$ is the thermal voltage ($kT/q$), also in this equation the $V_{ds}$ dependence of $I_d$ is neglected.

In [31], design of analog decoder in subthreshold region is discussed. The paper discusses the impact of DIBL, short channel effect, bulk bias voltage on the performance of MOS in subthreshold region. It also addresses the sizing of MOS based on current (power) requirements. Due to small voltage headroom, generally current mode operations are achieved in subthreshold region. This also facilitates low power designs. Andreas G. Andreou [32] has
implemented current controlled current conveyor which are used for silicon retina system design. Further, the $g_m$ efficiency is highest in subthreshold region and hence design of low power op-amps becomes convenient, but the speed of opamps is compromised. In [33], an ultra-low power op-amp operating at 0.5V supply voltage is discussed. A detailed study of MOS operation and modeling can be studied in [34].

3.2 Op-amp based architectures:

Whether it is DT or CT SDM, op-amps are the building blocks of both SDMs. The most common way to reduce the power consumption is to employ a cascade-of-integrator-feedback [35] which avoids a power-hungry summer amplifier. In [36], swing reduction technique has been considered which relaxes the requirements of slew rates of op-amps (SR is proportional to biasing current) and hence reducing the power consumed. Paper [37] mentions an interesting method, by selecting impedance levels of second and subsequent op-amp integrator much higher than that of first order, improves the power consumption but at the expense of larger chip area.

Another way explored in [38] [39] is to reduce the number of op-amp integrators by double sampling integrators. Apart from it, since multibit SDM needs additional Dynamic Element Matching (DEM) circuitry, single bit modulator architecture is preferred due to its simple circuit and lesser power load.

On circuit level, the improvement can be carried out at both integrating blocks and the comparator circuit. However, since clocked comparators do not lead to any static power dissipation, the prime focus of most of the work is on op-amp based integrators. In [40], class AB-op-amp is used to reduce the power consumption and for larger swing operation with incremental ADC architecture. Hanqing Wang in [41], has designed fourth order SDM using half delay integrators and switched-shared opamps. One very interesting way of reducing power is employed by [42], which utilizes assisted opamps in the design.

3.3 Passive loop filter architecture:

The most interesting option to reduce power is to implement the loop filter using only passive elements hence eliminating all opamps from the architecture. Hence the only power dissipating elements are comparator and feedback DAC which can be clocked to reduce the power
consumption. Especially in sub-nanometer technology the idea of passive filter is very lucrative. In papers [43-49], the sigma delta ADC employs passive loop filters.

However, this architecture is suitable mainly for medium resolution-low speed applications. The reason of this limit has been discussed in subsequent chapter. One of the major limitation of this architecture is lower loop gain and the attenuation of both error signal. Due to this the design burden is on comparator, as it is the only active component to provide loop gain, further it should have very low offset to detect small error signal. To overcome this problem, a preamplifier (sense amplifier) can be introduced before the latch.

The passive filter can be implemented either by using switched-capacitors based filters or RC-filters. The advantage of using switched-capacitors based filter is that a processing gain can be achieved to improve the performance. However, the design needs to simulate switches and non-overlapping clock signals, which are challenging to implement in subthreshold region. On the other hand, RC-filter design is very simple to implement and hence is more viable to design in ultra-low voltage case.

To the best knowledge of author, there has been no attempt to design passive sigma delta ADC in subthreshold region and an attempt to implement the same at 0.5V in 180nm CMOS technology is carried out in this work.

3. 4 Hybrid architecture:

In [50-52], the loop filter is designed using combination of both passive and active integrators. In [50] and [51], a fifth order loop filter is implemented in 0.25um and 0.18um technology respectively, wherein second and fourth integrators are designed using passive components. In this way, the attenuated error signal (by passive integrator) is amplified by active integrator which relaxes the design of comparator. Also, the noise introduced by passive integrator is shaped by active integrators which improves the SNR of ADC.

Table 2 summarizes the performances of various passive and hybrid integrator topology based ADCs.
Table 2: Comparison of different passive and hybrid integrator topology based ADCs

<table>
<thead>
<tr>
<th>Paper</th>
<th>Architecture</th>
<th>Technology</th>
<th>Supply voltage (V)</th>
<th>Loop filter order</th>
<th>BW (Hz)</th>
<th>Sampling freq. (Hz)</th>
<th>SNDR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[38]</td>
<td>Passive switched capacitor SDM (PSC)</td>
<td>1.2um</td>
<td>3.3</td>
<td>2</td>
<td>20k</td>
<td>10M</td>
<td>67</td>
</tr>
<tr>
<td>[39]</td>
<td>PSC-SDM</td>
<td>0.13um</td>
<td>1.5</td>
<td>2</td>
<td>100K</td>
<td>104M</td>
<td>74.1</td>
</tr>
<tr>
<td>[40]</td>
<td>PSC-SDM</td>
<td>0.18um</td>
<td>1</td>
<td>2</td>
<td>100K</td>
<td>100M</td>
<td>73.6</td>
</tr>
<tr>
<td>[42]</td>
<td>RC-integrator</td>
<td>0.13um</td>
<td>1.2</td>
<td>2</td>
<td>1M</td>
<td>200M</td>
<td>52.8</td>
</tr>
<tr>
<td>[43]</td>
<td>PSC-SDM</td>
<td>0.5um</td>
<td>2.5</td>
<td>2</td>
<td>3K</td>
<td>1.024M</td>
<td>57.6</td>
</tr>
<tr>
<td>[44]</td>
<td>RC-integrator</td>
<td>0.5um</td>
<td>5</td>
<td>2</td>
<td>5K</td>
<td>10M</td>
<td>48</td>
</tr>
<tr>
<td>[45]</td>
<td>Hybrid</td>
<td>0.25um</td>
<td>1.5</td>
<td>5</td>
<td>2M</td>
<td>150M</td>
<td>63.4</td>
</tr>
<tr>
<td>[46]</td>
<td>Hybrid</td>
<td>0.18um</td>
<td>1.8</td>
<td>5</td>
<td>2M</td>
<td>128M</td>
<td>60.26</td>
</tr>
<tr>
<td>[47]</td>
<td>Hybrid</td>
<td>0.065um</td>
<td>1.2</td>
<td>2</td>
<td>2M</td>
<td>400M</td>
<td>60.7</td>
</tr>
</tbody>
</table>
As discussed in previous chapter, the basic architecture of sigma delta ADC comprises of loop filter, comparator and feedback network built using DAC. In most of the sigma delta ADC architecture, the loop filter is designed using active integrator blocks. Hence operational amplifier is one of the basic building block of overall ADC design. Commonly the comparators are clocked-comparator and the DAC is realized using inverters for single bit quantizer based ADC, hence the power dissipated in these circuits is low and can be reduced further by using lower clock frequency. Hence, power hungry opamps limit the low power design requirements. Another approach to limit the power would be to reduce supply voltage to subthreshold level. But in sub-nanometer CMOS technology, the design of op-amp with large open loop gain and unity BW is a challenge which aggravates further in subthreshold region. It has already been studied that the poor performance of op-amp in terms of DC gain, UBW, slew rate; degrades the performance of sigma delta ADC [53].

In recent approach, the loop filter has been implemented based on passive integrator instead of active integrator as discussed in last chapter. Though this architecture helps in reducing the power, the cost is inferior resolution of ADC. A comparison study of both active and passive integrator (1st order with Fs = 10MHz) was performed using MATLAB Simulink and it showed 20dB improvement when active integrator used.

![Figure 6 : Comparison of Active and Passive first order Sigma Delta Modulator](image)
In previous chapter, various passive integrator based SDMs were studied. In this work the [49] architecture of modified second order loop filter is studied and employed. In [49,54] the analysis of first and second order passive loop filters using circuit analysis method has been performed, to determine STF and NTF of SDM. In [49] the similar analysis is carried out but by eliminating the current term through R2 (in figure 10) for simplicity, in this work; this analysis is re-visited and the design of subthreshold region operated passive sigma delta is carried out in this work.

In [49] the analysis is carried out using Mathematica tool, whereas for an easy and complete approach, the Signal Flow Graph (SFG) method is utilized instead to find $V_{out}$ in terms of $V_{in}$, $V_{qe}$ (Quantizer noise voltage) and $V_{int}$ (internal node voltage, for loop filter).

First, the SFG analysis is carried out for 1st order passive sigma delta to establish the method by comparing it with the results obtained in [54].

4.1 ANALYSIS OF PASSIVE SIGMA DELTA ADC USING SIGNAL FLOW GRAPH METHOD:

a. First order passive sigma delta ADC:

![Block diagram of first order passive Sigma Delta ADC](image)

The linear equivalent model of above circuit is shown below: The inverter is realized using gain of ‘-1’ and the sample and hold circuit with unity gain block; like in Baker’s book [54]. It is also assumed that there is no aliasing due to sampling and the filter characteristic obtained by loop is sufficient to shape out.
Figure 8: Linear equivalent model of first order passive Sigma Delta ADC

Writing KCL at nodes:

\[ \frac{v_{in}-2v_{int}-v_{out}}{R_1} = sC_1 * V_{int} \] …… (1.a)

\[ V_{int} + V_q = V_{out} \] …… (1.b)

Using equations (1.a) and (1.b) the SFG of 1st order P-SDM can be drawn as shown below:

Figure 9: Signal Flow Graph model of 1st order (also valid for 2nd order)

Where,

\[ g_1 = \frac{1}{R_1} \]
\[ g_2 = \frac{1}{sC_1} \]
\[ g_3 = 1 \]
\[ g_4 = 1 \]
\[ g_5 = 1 \]
\[ g_6 = -\frac{2}{R_1} \]
\[ g_7 = -\frac{1}{R_1} \]

On solving SFG we have,

\[ STF = \frac{1}{1 + (sC_1R_1)} \]

\[ NTF = \frac{(sC_1R_1)}{1 + (sC_1R_1)} \]
\[ \text{DTF} = \frac{-2}{1 + (sC_1R_1)} \]

Which are same as obtained in [54].

**b. Second order passive sigma delta ADC (as proposed in [49]):**

The SFG analysis is then extended to obtain STF, NTF and DTF of II\textsuperscript{nd} order P-SDM proposed by [49]. The block circuit diagram and linear equivalent model of it are as shown in figures below:

![Block Diagram](image1)

**Figure 10 : Block diagram of second order passive Sigma Delta ADC**

![Linear Equivalent Model](image2)

**Figure 11 : Linear equivalent model of second order passive Sigma Delta ADC**

The KCL equations at different nodes can be written as:

\[ \frac{V_{in}-2V_{int1}-V_{out}}{R_1} + \frac{V_{int2}-V_{int1}}{R_2} = sC_1 * V_{int1} \quad \ldots \ldots (2.a) \]

\[ \frac{V_{in}-2V_{int1}-V_{out}}{R_1} + \left( \frac{1}{(1+sC_2R_2)} - 1 \right) * \left( \frac{V_{int1}}{R_2} \right) = sC_1 * V_{int1} \quad \ldots \ldots (2.b) \]
\[
\frac{1}{1 + s C_2 R_2} \cdot V_{int1} + V_q = V_{out} \quad \text{.......... (2.c)}
\]

The equivalent SFG is similar to fig (9) with,

\[
g_1 = \frac{1}{R_1} \quad g_2 = \frac{1}{s C_1} \quad g_3 = \frac{1}{(1 + s C_2 R_2)} \quad g_4 = 1 \quad g_5 = 1
\]

\[
g_6 = \frac{-2/R_1 - \frac{-s C_2}{(1 + s C_2 R_2)}} \quad g_7 = -\frac{1}{R_1}
\]

On solving SFG, we have

\[
\text{STF} = \frac{1}{1 + (s C_1 R_1)(1 + s C_2 R_2)}
\]

\[
\text{NTF} = \frac{(s C_1 R_1)(1 + s C_2 R_2)}{1 + (s C_1 R_1)(1 + s C_2 R_2)}
\]

\[
\text{DTF} = \frac{(s C_2 R_1) + 2 \cdot (1 + s C_2 R_2)}{1 + (s C_1 R_1)(1 + s C_2 R_2)} \cdot \frac{1}{(1 + s C_2 R_2)}
\]

At low frequency, the DTF can be simplified as below:

\[
\text{DTF} = \frac{2}{1 + (s C_1 R_1)(1 + s C_2 R_2)}
\]

Which shows, like first order loop filter, the DTF is twice or 6dB higher than STF but both have second order low pass filter characteristic as expected.

The NTF also shows second order high pass characteristic, however both zeros are not at origin which is the case in ideal sigma delta modulator. To achieve the 40dB high pass characteristic for noise at lower frequency, the value of both C2 and R2 should be high. The exact impact of each passive component on STF and NTF was studied using MATLAB before choosing their final values.
Figure 12: STF and NTF plots with $R_2 = 1$M ohms, $C_1 = C_2 = 10$pF
Figure 13: STF and NTF plots with $R_1 = 1\text{M ohms}, C_1 = C_2 = 10\text{pF}$
Figure 14: STF and NTF plots with $R_1 = R_2 = 1\text{M ohms}, C_2 = 10\text{pF}$
Figure 15: STF and NTF plots with $R_1 = R_2 = 1\text{M ohms, } C_1 = 10\text{pF}$
Finally, $R_1 = R_2 = 1\text{Mohms}$ and $C_1 = C_2 = 10\text{pF}$ values were chosen for the passive components. The Bode plot of STF and NTF with these values is drawn below:

![Bode Diagram](image)

**Figure 16:** Final STF and NTF plots with $R_1 = R_2 = 1\text{M ohms}$, and $C_1 = C_2 = 10\text{pF}$
4.2 COMPARISON OF PROPOSED SFG ANALYSIS WITH REFERENCE PAPER

To compare both methods, the STF and NTF were plotted using MATLAB script. The comparison was done for final design values of passive elements used in A. Roy’s work on passive SDM [49] and was later extended for final values used in this work.

Figure 17: Comparison of STF and NTF obtained using proposed SFG method and reference paper method for $R_1 = 50e3$ ohms, $R_2 = 1e6$ ohms and $C_1 = C_2 = 10e-12$ F
From above plots, it can be observed that the roll-off for STF obtained from Angsuman Roy’s work on passive SDM [49] is 20dB/dec, however STF obtained from proposed SFG method shows roll-off of 40dB/dec which is in accordance with number of state variables present in system.

For lower values of R1, both STF results in nearly equal attenuation at sampling frequency; but for higher value of R1 the difference is prominent and shows that proposed SFG method gives better understanding of STF and NTF over the one derived in [49].

4.3 SYSTEM LEVEL MODELING USING MATLAB SIMULINK:
After deciding the passive components values, a full system level simulation was carried out using MATLAB Simulink. Since the pressure sensor is differential in nature, the PSDM of [49] is modified to differential inputs architecture.

Fig.19 shows the Simulink model of PSDM implemented. Here, the input sinusoidal signal is first converted into differential pair of inputs and fed to the loop filter implemented using
R-C network (shown in figure 20). The comparator is implemented using relay block and the DAC is modeled using an inverter. Since the system is differential, and in practice the comparator can be designed fully differential, the inverter can be avoided by using out of phase outputs. However, in Simulink since relay gives a single ended output, the differential part is taken care by inverting the output before feeding to INDP (DAC input for positive terminal). The memory cell in model is added to break the algebraic loop in Simulink solver, otherwise it would give an error.

Figure 19: Simulink model of II\textsuperscript{nd} order Passive SDM ADC

Figure 20: Loop Filter for II\textsuperscript{nd} order Passive SDM ADC
One of the major advantages of fully differential ADC in terms of design is that there is no need of any reference voltage generation for comparator, hence any band gap reference circuit is not needed.

The differential output data is recorded in an array and post processing is performed using MATLAB code to analyze the spectrum. The spectrum of output signal is as shown in figure 21.

![Output spectrum of Passive SDM for fin=1kHz and vin=2*180mV (differential)](image)

**Figure 21**: Output spectrum of Passive SDM for fin=1kHz and vin=2*180mV (differential)

### 4.4 IMPACT OF NON-IDEALITIES:

The source of non-ideality can be a.) comparator b.) Resistor and Capacitor and c.) the jitter present in clock signal. In this work, the impact of first two is studied.
a. **Non-ideality of Comparator:**

The comparator is a vital element of passive SDM, and any non-ideality present in terms of hysteresis or offset deteriorates the SNR performance of SDM. The definitions of both hysteresis and offset voltage can be referred in application note of comparator by STMicroelectronics [55].

For modeling purpose, the hysteresis of comparator is simulated by adjusting switch ON-OFF point of relay block. The impact of hysteresis on SNDR can be seen in figure below.

![Noise spectrum for various Hysteresis levels](image)

**Figure 22 : Noise spectrum for various Hysteresis levels**

b. **Non-ideality of Resistor and Capacitors:**

The resistors and capacitors implemented in CMOS technology can show variation over process corners. Assuming a variation of ±10%, the impact of this variation on spectrum can be studied. First, the STF and NTF plots are analyzed, and it can be seen that, the variation in NTF is not very high as R-C values vary, however variation in STF is relatively higher. The STF attenuation at +10% variation is which supports better SNDR performance as even observed from the system level simulation (shown in fig.23).
Figure 23: STF and NTF v/s R-C values variation

Figure 24: Noise spectrum v/s R-C values variation
Chapter 5
Circuit Level Implementation

The passive sigma delta ADC is simulated in Cadence environment using 180nm CMOS technology SCL, ISRO pdk files. This process is 3 metal layers process with another top level metal layer available in addition that can be used for supply lines and PMOS and NMOS with 1.8V and 3.3V voltage levels, it also supports native NMOS transistor. The process also supports high-resistivity poly resistors and MIM capacitors. Both schematic and layout level simulations are performed to study the performance of passive sigma delta ADC.

The basic schematic of II\textsuperscript{nd} order Passive SDM ADC is as shown below. The final values of all passive components are decided from the MATLAB Simulink level simulation, as discussed in previous chapter. The feedback inverter (DAC) is not needed, as out-of-phase output signals are fed to the loop filter. Another important thing to notice is absence of any reference voltage in circuit which reduces the complexity further.

Figure 25 : Block Level schematic diagram of II\textsuperscript{nd} order Passive SDM ADC
a. The clocked comparator block:

The most important block of sigma delta ADC is the comparator circuit. Even if loop filter is designed perfectly, a poor performance of comparator can degrade the resolution of ADC. From previous chapter, it is evident that the non-ideality i.e. hysteresis in this case should be limited to tens of µV; so that the noise spectrum of ADC is not hampered. The interesting thing to note here is due to averaging of multiple samples there is an inherent relaxation on comparator’s performance.

There have been several comparator designs proposed in past for sigma delta ADC. However, since in this work, the comparator should work under subthreshold region, the design of moderately high frequency comparator is challenging.

In general, the design of comparator is based on double tail current [56], here the operating voltage is reduced by separating the latching and input stages, thus reducing the stacking w.r.t. conventional comparator. However typically the supply voltage is still higher than Vt of transistor. In [57-59], the low voltage operation is achieved by boosting supply voltage or clock voltage; in these circuits, a few additional circuits are therefore needed like the level shifter and voltage booster. Paper [60] describes the design of a comparator using native NMOS transistor (which doesn’t have any threshold adjust implant and hence has very low threshold voltage). Rail-to-rail input range is achieved and the conventional comparator circuit is modified such that leakage current of native transistors has no impact on the functionality of the comparator. This performance is achieved however at increased process cost. Junjie Lu [61] has introduced a very interesting method of offset reduction by controlling the bulk terminal of input transistors, where the control signal is generated using charged pump circuitry.

Papers [62-64] have utilized bulk terminal as input stage instead of gate terminal. Pun et. al. has implemented sigma delta ADC at 0.5V in 180nm, the comparator here is designed using bulk driven pre-amplifier stage and the latch is implemented using bulk-inverter. Thus, this technique needs triple well technology. The results of comparator are not
included in paper, hence are not used here for comparison. In [63] positive feedback by cross-coupled NMOS load is used for comparator functioning. In [64], the comparator is designed in-line with the design proposed in [63], but additionally an offset trimmable circuit is implemented to lower the input offset. Further, to improve the operating frequency range, the gate voltage of cross-coupled MOS(s) is boosted, with this the comparator is found functional up to 200MHz.

Here the comparator is chosen to be bulk-input driven. Though the results of [62] are not reported, the design seems simple and suitable due to less stacking. Since the SCL CMOS 180nm process is nwell supported, the input stage is chosen to be PMOS-bulk, this also helps in reducing the input referred noise. Further, the bulk-driven inverter latch of [62] is not possible and is replaced with conventional gate driven inverter latch. It can be argued that the speed of comparator is mainly governed by the speed of latch, thus the gate-driven inverter latch also seems suitable in this context, with input stage acting as pre-amplifier stage. The circuit diagram of proposed comparator is as shown in figure 26.

When clock signal is high, M2a and M2b reset the outputs to 0V. During Vclk=0, both M1a and M1b conduct and their strength depends on the respective bulk voltages. Any differential voltage results in higher pull up strength of either M1a or M1b, the regenerative action of back-to-back connected inverter then results into differential comparator output. As discussed in chapter 3, any offset (or hysteresis) present, deteriorates the performance of the sigma delta ADC. Further, any input noise present at the comparator will also reduce the SNDR of ADC, hence the sizing of transistors is done accordingly.

The advantage of this circuit is that it has rail-to-rail input range, and is simple to implement. The speed of comparator can be improved by strengthening the latch or increasing the size of input PMOS (thus increasing pre-amplifier gain) but the power dissipation will also increase accordingly. Hence there is a trade-off between the speed and power consumption of comparator.
Figure 27 shows the simulation results of comparator for rail-to-rail input. For input offset/hysteresis measurement a ramp input is applied to positive terminal of comparator while negative terminal is kept at Vdd/2. The simulation results are plotted in figure 28. From figure 28, we can observe that there is some deadlock zone where the comparator output is not in accordance to the definition, this is due to the offset present.
The output waveform of ramp input can be translated to transfer curve to analyze the hysteresis present (as shown in figure 29). The figure just depicts the hysteresis phenomenon and is not plotted to the scale. Later, the comparator layout (shown in figure 30) was implemented and simulated using Calibre. The hysteresis was measured and compared with the schematic level results. Further, the simulations were conducted at different process corners and the result is tabulated below.
Figure 30: Bulk input Comparator layout

Table 3: Offset and hysteresis of comparator pre-n-post layout and at process corners

<table>
<thead>
<tr>
<th>Layout level</th>
<th>Hysteresis(µV)</th>
<th>Offset voltage (µV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schematic level</td>
<td>2µ</td>
<td>1µ</td>
</tr>
<tr>
<td>Layout level</td>
<td>ss-</td>
<td>180µ</td>
</tr>
<tr>
<td></td>
<td>tt-</td>
<td>60µ</td>
</tr>
<tr>
<td></td>
<td>ff-</td>
<td>120µ</td>
</tr>
</tbody>
</table>

Table 4: Comparison of designed comparator with literature
<table>
<thead>
<tr>
<th>Paper</th>
<th>Comparator Design Technique</th>
<th>Process Technology</th>
<th>Supply Voltage (V)</th>
<th>Offset Voltage (V)</th>
<th>Frequency (Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[56]</td>
<td>Double-tail-Dynamic</td>
<td>180nm</td>
<td>0.8</td>
<td>7.8m</td>
<td>2.4G</td>
</tr>
<tr>
<td>[57]</td>
<td>Novel-track-n-hold with clock signal doubler</td>
<td>180nm</td>
<td>0.6</td>
<td></td>
<td>2M</td>
</tr>
<tr>
<td>[58]</td>
<td>Temporarily boosting supply voltage</td>
<td>65nm</td>
<td>0.5</td>
<td>12.9m</td>
<td>1.2G</td>
</tr>
<tr>
<td>[59]</td>
<td>Supply boosted</td>
<td>500nm</td>
<td>1.0</td>
<td>4.1m</td>
<td>6.5K</td>
</tr>
<tr>
<td>[60]</td>
<td>Native NMOS</td>
<td>130nm</td>
<td>0.5</td>
<td>9m</td>
<td>-</td>
</tr>
<tr>
<td>[61]</td>
<td>Time-Domain Bulk-Tuned Offset Cancellation</td>
<td>500nm</td>
<td>5</td>
<td>50.57µ</td>
<td>200K</td>
</tr>
<tr>
<td>[62]</td>
<td>Bulk driven input stage and Cross-coupled load</td>
<td>180nm</td>
<td>0.8</td>
<td>10µ</td>
<td>10M</td>
</tr>
<tr>
<td>[63]</td>
<td>Bulk driven input stage, boosted Cross-coupled load and offset trimming</td>
<td>180nm</td>
<td>0.5</td>
<td>200µ</td>
<td>200M</td>
</tr>
<tr>
<td>This work</td>
<td>Bulk driven input stage, and conventional latch</td>
<td>180nm</td>
<td>0.5</td>
<td>90µ</td>
<td>10M</td>
</tr>
</tbody>
</table>

b. Latch for NRZ feedback:

The output of comparator is available only during Vclk=0 phase, when clock is high; the comparator output is always low. Hence to provide a Non-Return-to-Zero type DAC feedback to the loop filter, a latch is needed. The timing of latch cock is adjusted such that it captures the information during Vclk=0 period correctly. The details of clock signal for latch are discussed later in this chapter.
The latch is designed using a NAND gate topology, the input to latch is comparator’s differential output followed by buffers. The working principle of NAND latch can be found in any digital logic circuit book. The schematic of NAND latch is drawn below.

![Figure 31: NAND based latch](image)

In low voltage design, there have been different design logics say, domino, CMOS, etc. that have been proposed. Further the bulk terminal of the MOS is used to adjust the threshold voltage such that logic gates are made functional at low supply voltages [65]. Here CMOS logic design is used for its robustness. Also, since there is only PMOS’s bulk terminal is available, only its threshold voltage can be adjusted. In DTMOS, the bulk is shorted with gate terminal of MOS and hence its threshold voltage gets adjusted, though the dynamic bulk biasing has advantage over STMOS, it needs a separate bias circuitry. Hence in this work DTMOS is considered.

The latch’s functionality was tested pre-and-post layout. In this report only one set of results have been reported.
Figure 32 : NAND based Latch layout

Figure 33 : NAND based Latch post layout performance
c. Clock signal for Latch:

As described previously, the comparator output (which is available during half the clock cycle) needs to be converted to NRZ format using a latch; for an additional clock signal is needed. The clock signal for latch is derived on-chip using the combinational circuits as shown figure 34.

![Figure 34: Schematic of clock signal generation for latch](image)

After schematic level testing, layout of same was implemented. The essential part to remember while making layout is bulk terminal connection. The result of latch clock signal, post layout is presented in figure 36. the post layout performance at ‘ss’ and ‘tt’ process corner was found as per need, however at ‘ff’ corner the rising edge of latch clock signal was not present during negative period system clock. The reason for this was the reduced rise and fall delay of inverter delay elements used in the block. This problem is however trivial and can be addressed by tuning delay elements.
The hierarchal level simulation and layout was performed on comparator, latch and latch clock module (shown in figure 37 below). The performance was observed pre-and-post layout. The post layout result is plotted in figure 38.

Figure 35 : Layout of clock signal generation for latch

Figure 36 : Post layout results of clock signal generation for latch

d. Comparator + Latch + Latch clock system

The hierarchal level simulation and layout was performed on comparator, latch and latch clock module (shown in figure 37 below). The performance was observed pre-and-post layout. The post layout result is plotted in figure 38.
Figure 37: Post layout results of clock signal generation for latch

Figure 38: Post layout results of clock signal generation for latch
e. **Full Passive sigma delta ADC**

The loop filter is built using passive elements present in the SCL library. The resistor is implemented using HIPO–High Ohmic P-type Poly resistor with sheet resistance=1000Ω/sq. There are two terminals and three terminal resistors available in the library. The equivalent model of each of them with respective calculation can be found from foundry document (not referred here due to privacy). The two terminal shows absence of any parasitic capacitors or diodes w.r.t. poly and bulk and has been used in this design. For capacitors, MIM capacitor is used in design.

The passive sigma delta ADC is simulated for 10 cycles of input signals. The details on selection of runtime is discussed in Appendix 1. The error signal is monitored to determine the proper working of ADC. The frequency domain analysis is performed using the MATLAB script, included in Appendix 2. One of the important point to remember here is the sigma delta simulation generates lot of data points and hence strobe option of transient analysis is utilized here. All data points are recorded at the mid of clock period as the NRZ latch output remains stable at this time instance. The details of transient analysis setup can be found in cadence help menu.

The schematic level simulation was performed using SCL library passive elements. However, the layout of the full passive SDM is not implemented in this work since there was mismatch between the layout of resistors and MIM cap provided by foundry with the definitions (device parameter) provided in schematic level for same. Due to this the LVS and PEX were not possible. Hence for post layout condition, the passive components are replaced with schematic level passive elements available from foundry instead of their calibre equivalent and only MOS based blocks are replaced with their layout. Here only post layout performance is included. Figure 39 shows the performance of ADC at 1KHz (for test bench the freq is chosen as prime factor multiple though in accordance to standard practice for measurement of SNDR, however in case SDM this can be avoided too) for 360mV differential input. The SNDR and SNR obtained are 64.5 dB and 66.8 dB respectively.
The ADC performance was later evaluated for varying input signal amplitude to obtain the Dynamic Range (DR) of the passive SDM. Figure 40 shows variation of SFDR (it can be SNR or SNDR too) \( v/s \) the input signal amplitude. The DR achieved is 63.7dB.
The linearity of ADC can also be checked with ramp signal as input for conversion and a filter is used to obtain the ramp signal back from digital output of ADC. Figure 41 shows the performance of passive SDM for ramp signal input. The filter output shows a delay (signal in green colour), for comparison purpose this delay is eliminated (blue colour waveform). From following waveform, it can be observed that the output does not faithfully follows input ramp near the extremes of power rail (both $V_{dd}$ and GND). This is due to low loop gain value of passive SDM.

Figure 41 : SFDR v/s input signal amplitude at 1KHz input frequency

Further, the ADC was characterized for different input signal frequency and the FFT plot at each frequency is plotted to determine the SNDR and SNR. The performance was not evaluated at very sub KHz frequency as it consumes lot of simulation time. Figure 42 shows the ADC performance at different frequencies.
Figure 42: Passive SDM performance at different frequency

### Table 5: SNR and SNDR performance at different frequency

<table>
<thead>
<tr>
<th>Frequency (Hz)</th>
<th>SNDR (dB)</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1K</td>
<td>64.5</td>
<td>66.8</td>
</tr>
<tr>
<td>3K</td>
<td>63.9</td>
<td>65.9</td>
</tr>
<tr>
<td>5K</td>
<td>62.9</td>
<td>63.6</td>
</tr>
<tr>
<td>9K</td>
<td>65.01</td>
<td>65.01</td>
</tr>
</tbody>
</table>

Since, the post layout simulation including passive elements was not possible, the ADC is characterized for ±10% variation in the passive element’s values. This variation can be due to layout itself or process variations. The simulation was carried out for 3KHz input signal frequency and results are as shown in figure below. There is no significant variation is observed and the SNDR performance is best for ‘RC high’ (when both R and C values are higher than design values), which even supports the analysis conducted in chapter 4. The SNDR performance for each case is listed in table 6 below and the corresponding spectrum is plotted in figure 43.

### Table 6: SNR and SNDR performance at different RC product corner

<table>
<thead>
<tr>
<th>RC values</th>
<th>SNDR (dB)</th>
<th>SNR (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>61.7</td>
<td>65.1</td>
</tr>
<tr>
<td>Normal</td>
<td>63.9</td>
<td>65.9</td>
</tr>
<tr>
<td>High</td>
<td>64.3</td>
<td>66.7</td>
</tr>
</tbody>
</table>
Due to non-availability of monte variations setup, the random offset of comparator was not measured. However, in Simulink the impact of random offset on ADC performance was studied by randomizing the threshold for relay block (used as comparator). The mean value of zero and sigma equal to 15u (>15% of static offset found from cadence simulation) was set. The simulation was performed for 100 seeds and the worst case SFDR was around 65.5dB. A degradation of around 5dB w.r.t. simulation results obtained with no offset case.
In this work, the passive sigma delta ADC for ultra-low power and medium resolution applications is designed. Instead of conventional circuit level equations solving, to obtain the STF, NTF and DTF of passive SDM, a Signal Flow Graph (SFG) has been proposed here and the results obtained for first order passive SDM are verified with Baker’s work. The general approach of the analysis makes it suitable for any combinations of resistive and capacitive passive elements, unlike one proposed in [44] which defines STF and NTF for R1<<R2. This was verified and listed in chapter 4.

The block level performance of passive SDM was carried to derive the allowable variation in non-ideal performance of its building blocks. The circuit level performance was measured in terms of FoM and SNDR of ADC. The comparison study of SNDR and FOM w.r.t. referenced papers is tabulated below. For FOM calculation the formula mentioned in chapter 2 is used. The power dissipation was found to be only 4µW.

Table 7: Comparison of SNDR and FOM of various passive SDM

<table>
<thead>
<tr>
<th>Paper</th>
<th>Architecture</th>
<th>Technology</th>
<th>Supply voltage (V)</th>
<th>Loop filter order</th>
<th>BW (Hz)</th>
<th>Sampling freq. (Hz)</th>
<th>SNDR (dB)</th>
<th>FOM (fJ/step)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[38]</td>
<td>Passive switched capacitor (PSC-SDM)</td>
<td>1.2 µm</td>
<td>3.3</td>
<td>2</td>
<td>20k</td>
<td>10M</td>
<td>67</td>
<td>3417.5</td>
</tr>
<tr>
<td>[39]</td>
<td>PSC-SDM</td>
<td>0.13 µm</td>
<td>1.5</td>
<td>2</td>
<td>100K</td>
<td>104M</td>
<td>74.1</td>
<td>1539.2</td>
</tr>
<tr>
<td>[40]</td>
<td>PSC-SDM</td>
<td>0.18 µm</td>
<td>1</td>
<td>2</td>
<td>100K</td>
<td>100M</td>
<td>73.6</td>
<td>-</td>
</tr>
<tr>
<td>[42]</td>
<td>RC-integrator</td>
<td>0.13 µm</td>
<td>1.2</td>
<td>2</td>
<td>1M</td>
<td>200M</td>
<td>52.8</td>
<td>133</td>
</tr>
<tr>
<td>[43]</td>
<td>PSC-SDM</td>
<td>0.5 µm</td>
<td>2.5</td>
<td>2</td>
<td>3K</td>
<td>1.024M</td>
<td>57.6</td>
<td>1784.73</td>
</tr>
<tr>
<td>[44]</td>
<td>RC-integrator</td>
<td>0.5 µm</td>
<td>5</td>
<td>2</td>
<td>5K</td>
<td>10M</td>
<td>48</td>
<td>39062.5</td>
</tr>
<tr>
<td>[45]</td>
<td>Hybrid</td>
<td>0.25 µm</td>
<td>1.5</td>
<td>5</td>
<td>2M</td>
<td>150M</td>
<td>63.4</td>
<td>558.47</td>
</tr>
</tbody>
</table>
From above comparison table it can be observed that the presented work has excellent FOM (after [42]) while operating in subthreshold region.

This comparison study can be extended to Boris Murmann database of ADCs [66]. Here only continuous time SDM ADCs are retained for comparison.

<table>
<thead>
<tr>
<th></th>
<th>Hybrid</th>
<th>0.18µm</th>
<th>1.8</th>
<th>5</th>
<th>2M</th>
<th>128M</th>
<th>60.26</th>
<th>2670</th>
</tr>
</thead>
<tbody>
<tr>
<td>[46]</td>
<td>Hybrid</td>
<td>0.065µm</td>
<td>1.2</td>
<td>2</td>
<td>2M</td>
<td>400M</td>
<td>60.7</td>
<td>-</td>
</tr>
<tr>
<td>This work</td>
<td>RC-integrator</td>
<td>0.18µm</td>
<td>0.5</td>
<td>2</td>
<td>10K</td>
<td>10M</td>
<td>64.5</td>
<td>145.78</td>
</tr>
</tbody>
</table>

Figure 45: FOMW comparison using Boris Murmann’s ADC database
From above graphs, it can be observed that the passive SDM designed in this work has very competitive FOMW and FOMS performance compared to published literature.

From this design work, we can observe that the passive sigma delta ADC stands as a very promising option for ultra-low medium resolution applications.
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[44] F. Chen S. Ramaswamy B. Bakkaloglu " A 1.5 V 1 mA 80 dB passive \$\Sigma$\Delta$\Sigma$ ADC in 0.13 \$\mu\$ m digital CMOS process " <em>IEEE ISSCC Dig. Tech. Papers</em> vol. 5455 pp. 244-245 Feb. 2003.


[57] C. Fayomi, G. I. Wirth, D. Binkley and A. Matsuzawa, "An experimental 0.6-V 57.5-fJ/conversion-step 250-kS/s 8-bit rail-to-rail successive approximation ADC in 0.18µm CMOS," 2009 16th IEEE


[64] M. Mohammadi and K. D. Sadeghipour, "A 0.5V 200MHz offset trimmable latch comparator in standard 0.18um CMOS process," 2013 21st Iranian Conference on Electrical Engineering (ICEE), Mashhad, 2013, pp. 1-4.

Appendix 1

Simulation time for cadence environment

For frequency spectrum analysis of sigma delta ADC, very large numbers are generally needed. This can increase the simulation time exponentially. Here a comparison of spectrum with runtime equal to 10 cycles of input signals and N*Ts (N is typically 2^20 and Ts is sampling period) respectively is carried out to determine the suitable runtime for all CADENCE simulation.

<table>
<thead>
<tr>
<th>Runtime</th>
<th>10/fin</th>
<th>N*Ts</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>65.1231</td>
<td>64.4362</td>
<td>0.6869</td>
</tr>
<tr>
<td>SNDR</td>
<td>64.5923</td>
<td>64.1672</td>
<td>0.4251</td>
</tr>
</tbody>
</table>

From above table, it can be observed that there is hardly 0.5dB variation in characteristic parameters when runtime is reduced to ‘10/fin’, but the corresponding advantage in cadence simulation run is remarkable. All measurements are therefore performed for 10/fin period.
MATLAB Code to analyze spectrum and compute SNR and SNDR

clear all;
clc;

Fs=10e6;
Ts=1/Fs;
N=2^20-1;  %% number of samples
Ain=180e-3;  %% input amplitude
Ain2=180e-3;
fin=1e3;  %% input freq

sim('SDM_passive ',10/fin)

y=BS;

%%% FFT plot

L=length(y);
w=hann(L,'periodic');
y=y.*w.*2;

NFIT=L;
Y = fft(y,NFIT)/L;
f = Fs/2*linspace(0,1,NFIT/2+1);

Y_out=20*log10(2*abs(Y(1:NFIT/2+1)));
ang=angle(Y(1:NFIT/2+1));

% Plot single-sided amplitude spectrum.
figure(1)
semilogx(f,20*log10(2*abs(Y(1:NFIT/2+1)))-20*log10(2*abs(max(Y(1:NFIT/2+1)))))
grid on;
hold on;

------------------------------------------
fin_bin=ceil(fin*(NFFT/2+1)/(Fs/2));
fin_bin_signal=[fin_bin-1,fin_bin,fin_bin+1];
harmonics_bin=ceil(3*fin*(NFFT/2+1)/(Fs/2));  //higher harmonics can also be considered

BW=10e3;
BW_bin=ceil(BW*(NFFT/2+1)/(Fs/2));
signal_power = 0;
total_power = 0;
for k=1:BW_bin
    total_power = total_power + (2*abs(Y2(k)))^2;
end

signal_power=(2*abs(Y2(fin_bin-1)))^2+(2*abs(Y2(fin_bin)))^2+(2*abs(Y2(fin_bin+1)))^2;
harmonics_power=(2*abs(Y2(harmonics_bin-1)))^2+(2*abs(Y2(harmonics_bin)))^2+(2*abs(Y2(harmonics_bin+1)))^2;
noise_power=total_power-signal_power;
noise_power1=total_power-signal_power-harmonics_power;
sndr=10*log10(signal_power)-10*log10(noise_power)

snr=10*log10(signal_power)-10*log10(noise_power1)