Clocking

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Need for clocking

- Need to sequence Operations
- Need to synchronize various paths
Sequencing Elements

- **Latch**: Level sensitive
  - a.k.a. transparent latch, D latch

- **Flip-flop**: edge triggered
  - a.k.a. master-slave flip-flop, D flip-flop, D register

- **Pulsed Latch**: A latch with a very narrow transparent window
Latch: Opaque state
Latch: Transparent

\[ t_{dq} = ? \]
Latch setup: Transparent to Opaque

\[ t_{\text{setup}} = ? \]
\[ t_{\text{hold}} = ? \]
Latch hold: Transparent to Opaque

$t_{\text{setup}} = \, ?$
$t_{\text{hold}} = \, ?$
Flop/Latch characterization

Figure 1. Definitions of setup and hold times.

FIG 7.40 Flip-flop setup and hold times
Flip-flop is built as pair of back-to-back latches.
Sequencing

Flip-Flops

2-Phase Transparent Latches

Half-Cycle 1

Pulsed Latches
Contamination and Propagation Delays

Combinational Logic

A → Y

Flop

clk

D → Q

Latch

clk

D → Q
Max-Delay: Flip-Flops

\[ t_{pcq} + t_{pd} \leq T_c - t_{setup} \]
Min-Delay: Flip-Flops

\[ t_{ccq} + t_{cd} \geq t_{hold} \]
Timing Analysis

Delay mismatch causes clock skew
Clock skew's impact on max delay

\[ t_{pcq} + t_{pd} \leq T_c - t_{setup} - t_{skew} \]
Skew's impact on min delay

$t_{ccq} + t_{cd} \geq t_{hold} + t_{skew}$