A Power-Scalable RF CMOS Receiver for 2.4 GHz Wireless Sensor Network Applications

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***Abstract*—A power scalable receiver architecture is presented for low data rate Wireless Sensor Network (WSN) applications in 130nm RF-CMOS technology. Power scalable receiver is motivated by the ability to leverage lower run-time performance requirement to save power. The proposed receiver is able to switch power settings based on available signal and interference levels while maintaining requisite BER. The Low-IF receiver consists of Variable Noise and Linearity LNA, IQ Mixers, VGA, Variable Order Complex Bandpass Filter and Variable Gain and Bandwidth Amplifier (VGBWA) capable of driving variable sampling rate ADC. Various blocks have independent power scaling controls depending on their noise, gain and interference rejection (IR) requirements. The receiver is designed for constant envelope QPSK-type modulation with 2.4GHz RF input, 3MHz IF and 2MHz bandwidth. The chip operates at 1V V_{dd} with current scalable from 4.5mA to 1.3mA and chip area of 0.65mm^2.**

***Index Terms*—Power Scalable, Low Power Receiver, Wireless Sensor Networks, 2.4GHz Receiver**

I. Introduction

In the current paradigm of seamless connectivity ultra-low power RF receivers are attracting lot of attention among researchers. As we move to more applications for WSN, the modules need longer battery life. A power scalable WSN receiver can lower it's power consumption under favorable input conditions. Circuit topologies and system level architectures suitable for power scalable receivers have not been sufficiently explored in literature. In [1] the authors introduced power scaling for wireless receivers and explored such adaptability in VCOs. In [2] adaptability was applied to LNA with power scaled for varying input strength to get power-noise tradeoff. In [3] we introduced a power scalable front-end with LNA power being scaled for both noise and linearity. In this paper we present full receiver chain with power scaling applied to various blocks depending on varying performance requirements.

The trade-offs involved in the receiver blocks are enumerated in Section II with discussion on effect of noise and interference on demodulation. The methodology of arriving at the receiver specifications for a power scalable architecture is discussed in Section III. In Section IV we discuss how performance of various receiver blocks can be traded-off with power and architectures which allow the same. The chip results are discussed in Section V with conclusions in Section VI.

II. Power Scaling Motivation

Wireless receivers have traditionally been designed for the worst case input, i.e. minimum signal and maximum interference. However in actual operation the input conditions might be better, i.e. higher signal and lower/no interference. In such cases receiver performance can be relaxed to just meet a required SNR at the ADC input, for successful demodulation. The sub-blocks of a Low-IF receiver are summarized in Fig.1. From Fig.2 we see that the required performance (Gain, NF and IIP3) for a Zigbee receiver, based on input conditions (signal strength and interference), varies over a wide range. This leads to the possibility of power scaling. For gain scaling we already have VGA in the receiver chain. NF of the chain is set mainly by the LNA NF and gain; thus power scaling can be applied to LNA to save power in higher input strength condition. As the presence/strength of interference in any wireless channel is variable, the filtering requirement of the receiver can be variable. Thus power scaling can be applied to filter to save power in low interference conditions.

The Zigbee baseband signal is a sequence of chips (half-sine pulses). The ideal/high SNR signal needs to be sampled once per chip for successful demodulation as the only possible values of a chip are $\pm$ 1 represented as a positive/negative half sine pulse. However in presence of noise more samples are needed to get a good correlation for demodulation (Fig.3). Also more resolution (higher no. of bits) is needed for noisy inputs to ADC. High interference necessitates higher sampling

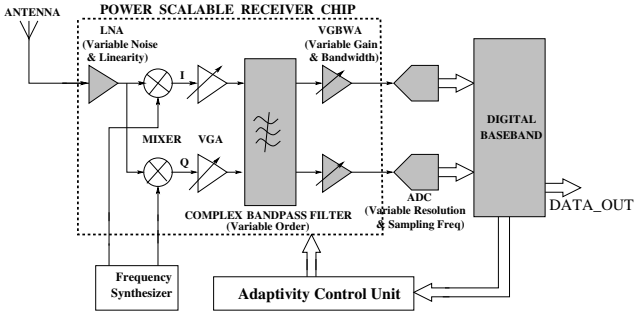


Fig. 1. Power Scalable Receiver System (The power scalable blocks are shaded)

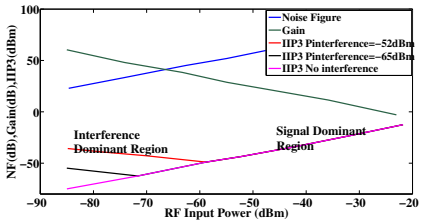
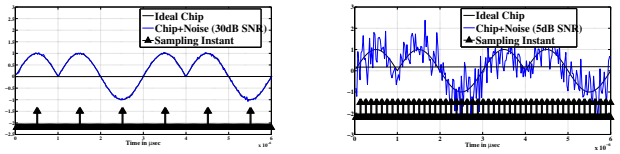


Fig. 2. Performance Requirement of Zigbee Receiver with Varying Input



(a) Chip with 30dB SNR AWGN (b) Chip with 5dB SNR AWGN

Fig. 3. Effect of Noise on Sampling Requirement for Demodulation in Zigbee

TABLE I
PERFORMANCE BUDGETING OF WSN RECEIVER

Parameters	LNA	Mixer	VGA	Filter	VGBWA	Total
Gain (dB)	4-15	1	0-38	2-6	8-20	15-80
NF (dB)	2-10	15	20	25-35	35-40	15-40
IIP3 (dBm)	0 to -10	5	5	10	10	-5 to -35

frequency in ADC to reduce aliasing. Thus power scaling can be applied to ADC by running it at lower resolution and sampling rate for clean input signals. The VGA driving the ADC will have relaxed settling time (bandwidth) requirement when ADC operates at lower sampling rate. This variability is used in the VGBWA for power scaling.

III. Power Scalable Receiver Specifications

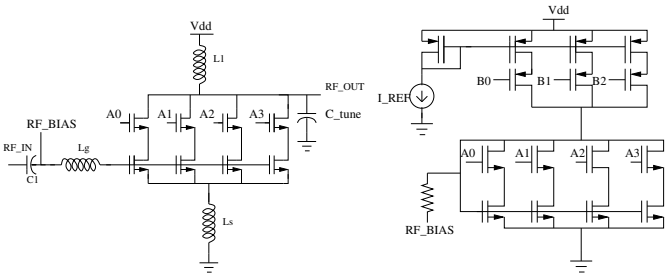
A power scalable receiver adapts its performance according to signal and interference levels, leading to power savings. How the specifications for a front-end vary as function of received signal condition has been discussed in [3]. With varying input conditions the receiver requires different NF, IIP3 and IR. The performance budget (Table I) of the receiver is calculated based on published results for Zigbee receivers and empirical equations, i.e. Sensitivity, Friis and Cascode IIP3 equations. From SNR vs. BER curves for QPSK modulation [4] we get 7dB SNR required at demodulator input for 10^{-3} BER. For gain calculation full scale ADC input is maintained at 800mV$_{pk-pk}$ differential. The input signal strength can vary in the range of -20 to -85 dBm.

IV. Receiver Architecture

A. Low Noise Amplifier-Mixer (LNAM)

The main requirement for LNA is to provide gain with low noise and reasonable linearity, as in-band blockers are present at LNA input. Being the first block in a receiver chain its performance, especially noise, impacts the receiver performance to a large extent. Mixer performance is not very critical if LNA gain is high. LNA power being a major component of receiver power substantial power savings is possible with power scaling LNA.

To reduce noise in LNA the input transistor g$_m$ should increase and to increase linearity the overdrive voltage should increase. These can be controlled independently by varying the width (W) and bias current (I) of the input transistor. The drain current noise voltage (V$_{ni}$) and the 3rd order intercept point voltage (V$_{IP3}$) of a transistor can be expressed as (1) & (2) where k=Boltzmann const, T=temperature, γ=noise coefficient



(a) Width Scaling in LNA (b) Current Scaling in Bias

Fig. 4. Power Scaling LNA Schematic with Replica Biasing

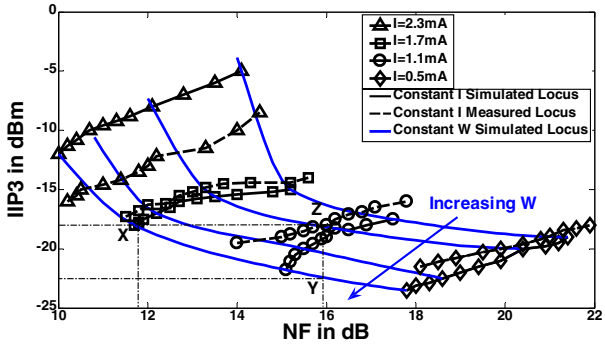


Fig. 5. Power Scaling Results (Measured & Simulated) for LNA-Mixer showing NF and IIP3 Variations with Locus of Constant I and W

and θ=fitting parameter$\simeq$(10^{-7}/t$_{ox}$)V^{-1}. Thus independent width and current control allows us to achieve any combination of required noise and linearity with lowest power for LNA.

$$V_{ni}^2 = \frac{4kT\gamma}{g_m} \propto \frac{1}{\sqrt{IW}} \quad (1)$$

$$V_{IP3}^2 = \frac{16}{3}\frac{I}{g_m\theta} \propto \frac{\sqrt{I}}{\sqrt{W}} \quad (2)$$

LNA architecture is inductively degenerated CS stage having a cascode transistor, with provision for variable width and current. The LNA schematic is shown in Fig.4. The input transistor's maximum width is W$_{opt}$ for NF$_{min}$ [5]. Width scaling is implemented by having transistors in parallel with binary weighted widths for the input transistor, with 4-bit (A3-A0) control and the cascode transistor as the switch. Bias is implemented as replica of the main LNA structure so that RF_BIAS can track width changes and keep I constant when W is varied. Current scaling is implemented by having transistors in parallel with binary weighted widths in the PMOS current mirror, with 3-bit (B2-B0) control. LNA current scaling range is 0.3-2.1mA at 1V, NF range is 2.1-6.5 dB, Gain range is -2 to 14 dB and IIP3 range is -20 to -5 dBm.

Figure 5 shows the graph of NF vs. IIP3 for the LNAM with varying W & I, which illustrates LNA power scaling strategy. The nature of these loci agrees with (1) & (2). Considering initial operation at pt. X (12dB NF and -18dBm IIP3); let input conditions change such that we can tolerate higher NF. With current control and fixed width we can reach pt. Y (16dB NF

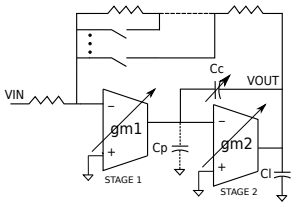


Fig. 6. VGBWA Block Diagram

and -23dBm IIP3); higher NF but lower IIP3. Having width control additionally allows us to operate at pt. Z (16dB NF and -18dBm IIP3); higher NF but same IIP3 as X, with a current savings of 35%. Thus independent W & I control allows trade-off of both noise and linearity for power.

B. Complex Bandpass Filter

Filtering is needed in the IF path of a receiver to remove in-band blockers. Higher order active filters lead to more IR with proportionally higher power. So there is direct relation between the IR required and power consumed in variable order filters.

In low-IF receivers, bandpass filters (BPF) are used to filter near-dc blockers and reduce DC offset and flicker noise. But traditional bandpass filters do not attenuate the image frequency which is possible using complex filters. Complex filter implementation is possible where I & Q signals are present and the two low-pass filters (LPF) of I and Q path are arranged in a cross-coupled resistive feedback which converts the LPF to a resultant BPF [6]. Recent trend of using complex filters in low-IF receivers has certain benefits as follows:

1. Image rejection without additional power overhead.
2. No capacitor at input of BPF reduces area requirement.

The complex BPF in the receiver has center frequency of 3MHz and can be operated as $1^{st}/2^{nd}/3^{rd}$ order filter using MUX with separate shutdown modes. The concept can be extended to higher order filters if more IR is required.

C. Variable Gain and Bandwidth Amplifier (VGBWA)

A VGA is needed after the filter to ensure full-scale input to ADC. As mentioned in Section II we can have a variable sampling rate ADC as part of power scalable receiver. When such an ADC operates at lower sampling rate it can tolerate slower settling on its sampling capacitors. The VGA driving this ADC can have variable output resistance (bandwidth) in addition to variable gain, which we call a Variable Gain and Bandwidth Amplifier. Next we discuss the dependence of the closed loop gain (G) and bandwidth (BW) of the VGBWA on input transconductance (g_m), which is set by the current.

The VGBWA uses two-stage miller compensated amplifier, with scalable current in both stages and variable compensation capacitor (C_c), placed in feedback with variable resistors (Fig.6). Current is scaled by switching additional transistors in parallel, using digital bits, with same gate bias which results in linear g_m scaling. BW can be maintained at different G settings by adjusting g_{m1} and C_c. Assuming no parasitic loading of 1^{st} stage, the closed loop BW, non-dominant pole (P_2) and Phase Margin (PM) can be approximately given by:

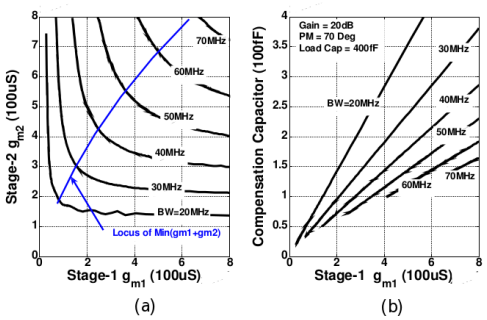


Fig. 7. Simulation Contours of (a) g_{m2} and (b) C_c with g_{m1}

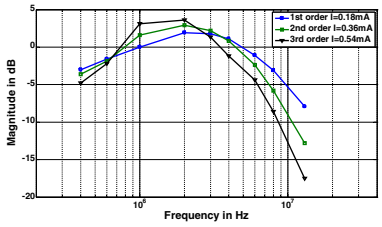


Fig. 8. Measured Filter Response of Variable Order Complex BPF

$$BW = \frac{g_{m1}}{2\pi C_c(1+G)} \tag{3}$$

$$P_2 = \frac{g_{m2}}{2\pi C_l}\left(\frac{C_c}{C_c + C_p}\right) \tag{4}$$

$$PM \simeq 90 - tan^{-1}\left(\frac{BW}{P_2}\right) \tag{5}$$

There are multiple values for g_{m1}, g_{m2} and C_c which will satisfy these equations but only one set will give minimum power. That can be found by putting a constraint of *minimize (g_{m1}+g_{m2})*. Fig.7 shows MATLAB simulations for the contours of g_{m2} and C_c vs. g_{m1} along with the locus of *Min(g_{m1}+g_{m2})*. G is selected based on receiver gain required and is set by switching feedback resistors. The BW and PM are calculated based on the acceptable settling time on the ADC input capacitors. Current setting for a desired BW is obtained from Fig.7(a). The g_{m1} from *Min(g_{m1}+g_{m2})* is then used in Fig.7(b) to find C_c to preserve the PM. The gain range for the VGBWA is 8 to 20 dB (3 bits), BW range is 15 to 45MHz and current scaling range is 0.1 to 0.17mA at 1V.

V. Results

A. Low Noise Amplifier-Mixer (LNAM)

The results for the LNAM are given together as only IF outputs were available. The LNAM maintains functional operation down to V_{dd}=0.7V though all measurements are for V_{dd}=1V. The measured results for the NF and IIP3 are highlighted previously in Fig.5. The power scaling strategy described in Section IV.A also holds for the measured results.

B. Complex Bandpass Filter

The measured frequency response is given in Fig.8.

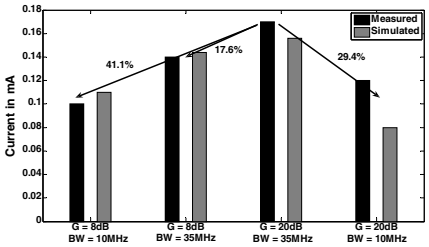


Fig. 9. Measured Current Consumption and Savings for VGBWA

TABLE II
POWER SCALABLE RECEIVER TEST CASES

Signal condition	Signal strength	Interference condition	Interference presence
Min	-50dBm	Min	Nil
Typ	-35dBm	Typ	Alternate Channel
Max	-20dBm	Max	Adjacent Channel

C. Variable Gain and Bandwidth Amplifier (VGBWA)

The current consumption and the percentage savings for the extreme settings (min & max G and BW) are shown in Fig.9. The measured BW (10-35MHz) is lower than the simulated BW (15-45MHz) due to additional layout parasitics.

D. Power Scalable Receiver

The power scalable receiver was tested for nine input conditions; combinations of three signal strength and three interference levels. The measured output signal power was maintained at -6dBm and SNR at 7dB (Section III). The settings of various power scaling blocks were adjusted according to input conditions to ensure similar signal and noise levels for ADC. The input conditions were classified as Minimum, Typical and Maximum whose values are given in Table II.

The measured current consumption values at 1V, for the different input conditions, is given in Fig.10. We achieve an average power savings of 62.5% for min-max signal variation and 25% for min-max interference variation. The receiver shows a sensitivity of -70dBm. Another option of power scaling available in our chip is by V_{dd} scaling. Operating the chip at 1.2V gives improved performance with higher power. The chip die photo and layout photo are given in Fig.11.

VI. CONCLUSION

In this paper we have demonstrated a power scalable receiver for 2.4GHz WSN applications. With measured/estimated input conditions this receiver gives significant power savings over traditional designs. Comparison with other recently published work is given in Table III. Similar analysis can also be carried out for baseband and PLL.

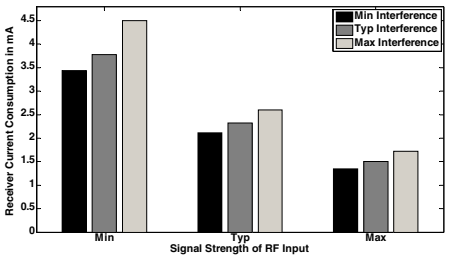
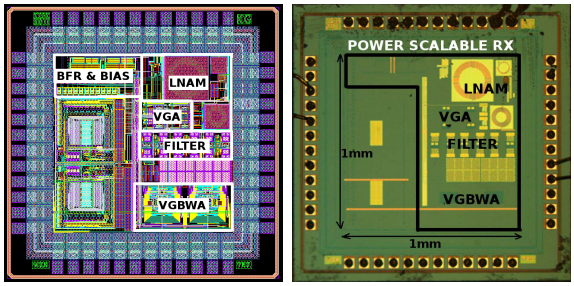


Fig. 10. Measured Current Scaling of Receiver for Different Input Conditions



(a) Chip Layout (b) Die Photo

Fig. 11. Power Scalable Receiver Chip Photo

TABLE III
COMPARISON WITH RECENTLY PUBLISHED LOW POWER RECEIVERS

Parameter	[7][1]	[8]	[2][2]	This work[3]
Technology	90nm	180nm	180nm	130nm
V_{dd}	1.35V	1.8V	1.8V	1.0-1.2V
Power	5.4mW	15.5mW	9 to 2.5mW	6.5 to 1.3mW
NF	7.5dB	6dB	8.8 to 16.5dB	12 to 40dB
IIP3	-10dBm	-11dBm	-19 to -31dBm	-8 to -35dBm
Sensitivity	NR[4]	-101dBm	NR[4]	-70dBm

[1] LNA, Mixer & 1^{st} order Filter [2] LNA, Mixer & TIA
[3] LNA, Mixer, VGA, Filter & VGBWA [4] NR - Not Reported

ACKNOWLEDGMENT

The authors would like to thank Department of Electronics & Information Technology, MCIT, Govt. of India for funding the project and the tapeout.

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