SRAM: Write and Read Path

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Write Operation
Write Noise Margin

\[ \beta_a >> \beta_p \]

Decrease Cell Vdd

Increase WL Vdd

Write Noise Margin
Dual VDD

Figure 26.1.1: Subarray configuration with built-in VCC MUX.

Figure 26.1.2: MUXing power supplies based on Read or Write.

Intel 65nm 3GHz, 70Mb, 1.1V supply (ISSCC 2005)
Floating VDD Writes

[Calhoun JSSC 2007]
Column circuit
Sense amp
Timing

CLK

WLn

PSn

Y, Bl

CAE
Timing Generation
Replica Based Self-Timing

[Amrutur, JSSC, Aug 1998]
Delay matching of two paths