Experimental Study on Substrate Noise Effects of a Pulsed Clocking Scheme on PLL Performance

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***Abstract*—In this brief, the substrate noise effects of a pulsed clocking scheme on the output spur level, the phase noise, and the peak-to-peak (Pk–Pk) deterministic period jitter of an integer-N charge-pump phase-locked loop (PLL) are demonstrated experimentally. The phenomenon of noise coupling to the PLL is also explained through experiments. The PLL output frequency is 500 MHz and it is implemented in the 0.13-μm CMOS technology. Measurements show a reduction of 12.53 dB in the PLL output spur level at an offset of 5 MHz and a reduction of 107 ps in the Pk–Pk deterministic period jitter upon reducing the duty cycle of the signal injected into the substrate from 50% to 20%. The results of the analyses suggest that using a pulsed clocking scheme for digital systems in mixed-signal integration along with other isolation techniques helps reduce the substrate noise effects on sensitive analog/radio-frequency circuits.**

***Index Terms*—Guard rings, jitter, mixed signal, phase noise, phase-locked loop (PLL), pulse clock, spur level, substrate noise, substrate, voltage-controlled ring oscillator (VCO).**

I. Introduction

THE NEED for more functionality in systems-on-a-chip is driving the integration of noise-sensitive analog/RF circuits along with noisy digital circuits. Digital circuits inject noise currents into the substrate during their signal transitions. Buffers in a clock distribution network of digital circuits usually have very large drive strengths and hence inject a significant amount of noise currents into the substrate [1]. A typical clock distribution network using a multilevel tree architecture [2] is shown in Fig. 1. The fast edge rate requirement from the final-stage clock buffers (see the local clock buffers and the second-level clock buffers in Fig. 1) makes them a dominant source of substrate noise injection.

Several techniques have been proposed in the past to mitigate substrate coupling effects, and they can be classified under two categories, i.e., the layout-based techniques and the circuit-based techniques. Some of the layout-based techniques reported are the deep n-well isolation [3], deep trench isolation, patterned ground shields [4], high-resistivity substrates, through-silicon-via-based physical isolation [5], and guard-ring structures [6]. Many of these layout-based techniques require additional process steps, and in some cases, they alter the performance of the circuits enclosed. The most common technique used by designers is the guard-ring structures (ohmic and well-type guard rings) around the sensitive blocks and noisy circuits. However, the isolation property of the guard-ring structures begins to saturate when the width of the rings is increased, and occupies a large area [7]. Hence, with the increasing substrate noise trend, using wider guard-ring structures alone is not an efficient solution as the isolation that they provide is limited and leads to saturation.

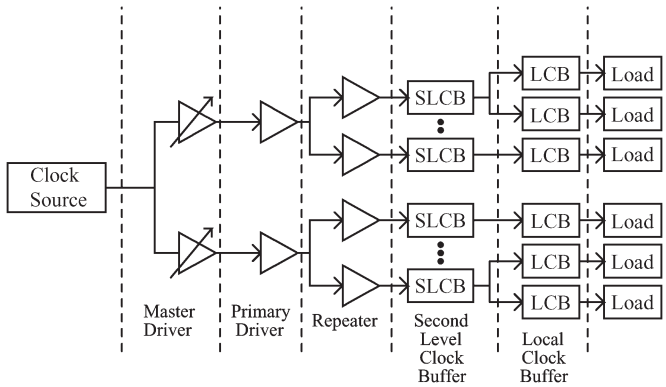

Fig. 1. Clock distribution network using a multilevel tree architecture used in synchronous digital systems.

The circuit-based techniques used to reduce substrate noise effects are approached in two ways: the modification in the analog part, in which fully differential circuit topologies with symmetrical matched layouts treat substrate noise as a common mode signal, and the modification in the digital part, in which the digital logic implemented with analog-based differential current-steering techniques, such as the folded source-coupled logic, reduce the power-supply noise-current spikes [8]. Both techniques require additional area and might not be practical for all applications.

The substrate noise effects on circuits can be simulated by including a substrate model along with the circuit net list. By analyzing the results, modifications can be made either in the circuit level or in the layout level to improve the circuit performance. However, the increased transistor count and very small minimum dimensions result in a huge substrate model, which makes it difficult to simulate within a reasonable time. A few works attempted to solve this problem through experimental demonstrations of substrate noise effects on sensitive circuits as a function of circuit parameters and through the use of different isolation techniques to provide guidelines in designing circuits with substrate noise immunity [9]–[11].

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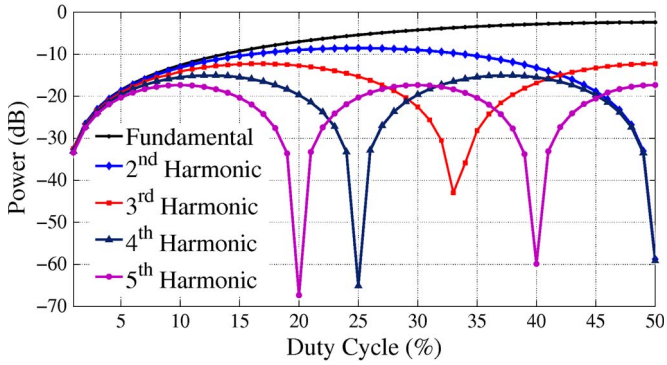


Fig. 2. Harmonic content of a 10-MHz clock signal as a function of its duty cycle.

Many high-performance processors have been routinely using pulsed clocking for over a decade [12]–[14] as it has the advantages of a reduced clock load, a low sequencing overload, skew tolerance, allowed time borrowing, and lesser energy consumption. The tradeoffs of using a pulsed clocking scheme are well understood and well articulated in standard digital textbooks [15]. Recently, it has been recognized that pulsed clocking can be also useful for low-power digital circuits [16].

In this brief, we experimentally demonstrate the effects of substrate noise generated from pulsed clock buffers on the performance of a phase-locked loop (PLL) (output spur level, phase noise, and jitter). The source and phenomenon of noise coupling is also explained through different experimental techniques. The results of the analyses suggest that using a pulsed digital clocking scheme for digital systems in a mixed-signal design helps in reducing its substrate noise effects. Fig. 2 shows the harmonic content of a 10-MHz clock signal and its dependence on the signal duty cycle. The lower power content of the fundamental harmonic of a pulsed clock signal and the low-pass filtering effect of the substrate (see Section IV) help reduce the substrate noise effects in mixed-signal integration.

The design details and the measured characteristics of individual PLL blocks are presented in Section II. The experimental setup for substrate noise injection and the mechanism of coupling to the PLL are explained with different experimental techniques in Sections III and IV, respectively. The results of the experimental analyses on the effect of substrate noise generated from a pulsed digital clock on the PLL performance are presented in Section V. Finally, the conclusions are presented in Section VI.

II. PLL Design

A type-II third-order integer-N charge-pump (CP) PLL, along with the substrate noise injector buffers shown in Fig. 3, is fabricated in the United Microelectronics Corporation 0.13-μm mixed mode and the 1.2/3.3-V 1P8M RF CMOS process. The PLL generates an output frequency of 500 MHz from a 1-MHz reference signal. The CP current is 50 μA. The loop filter (LPF) parameters are $R_z = 60$ kΩ, $C_z = 200$ pF, and $C_p = 15.2$ pF, and these are designed for a PLL bandwidth of 50 kHz and a phase margin of 60°. The current-steering CP architecture used in the PLL is designed to source or sink the programmable currents in the range of 3–100 μA from a reference current

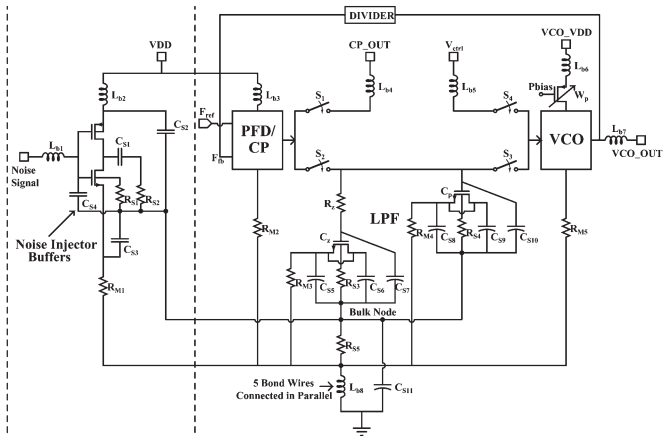


Fig. 3. Test bench. Type-II third-order integer-N CP PLL and noise injector buffers.

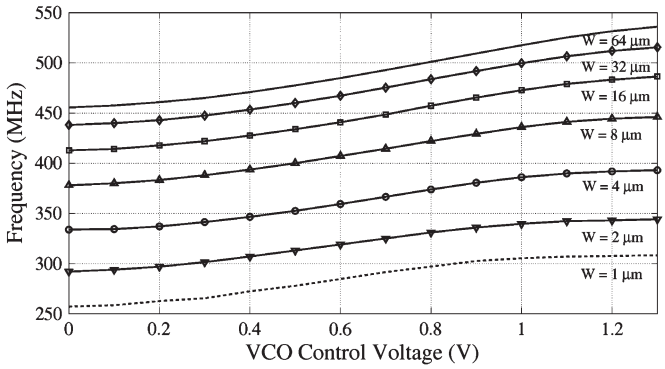


Fig. 4. Measured VCO transfer characteristics with different bias-current transistor widths W_p.

source of 10 μA. The LPF capacitors are implemented by using the gate capacitance of NMOS transistors to reduce the area occupied by large on-chip capacitors and hence are particularly susceptible to pick up substrate noise.

A five-stage pseudodifferential voltage-controlled ring oscillator (VCO) with varactor and bias-current tuning is used in the PLL, and it generates frequencies in the range of 455–536 MHz, achieving a gain of 72 MHz/V. Fig. 4 shows the measured VCO transfer characteristics with different bias-current transistor widths. A phase frequency detector (PFD) and a divider are implemented using standard digital logic circuits with a tristate dead-zone-free phase detector and down-counter architectures, respectively.

The PLL consumes a current of 4 mA (including output buffers) from a supply voltage of 1.2 V and achieves a phase noise of -104.5 dBc/Hz at an offset of 1 MHz from a 500-MHz carrier. Fig. 5 shows the measured phase noise characteristics of a 500-MHz signal generated by the PLL. The spur C in the phase noise characteristics is due to the periodic substrate noise of 5 MHz generated from the noise injector buffers, and spurs A and B are due to the background measurement activity.

III. Experimental Setup

Digital switching noise is generated on-chip by a chain of large-sized digital buffers (inverters) that have no guard rings around them. These buffers inject noise into the substrate

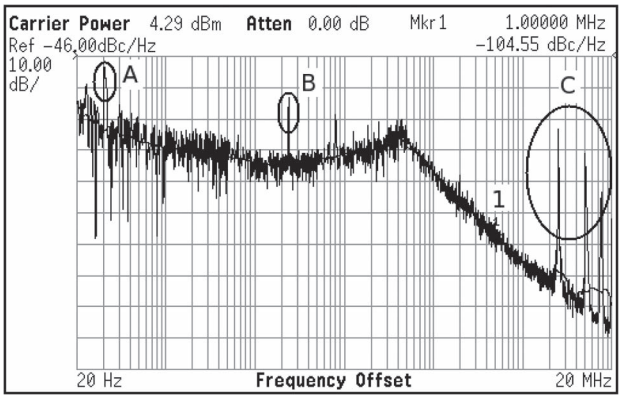
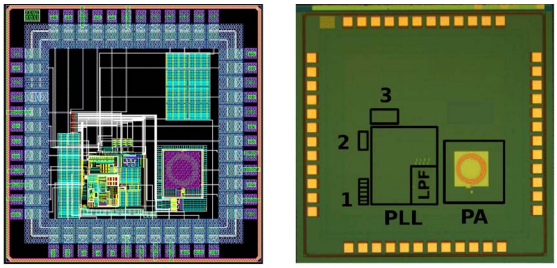


Fig. 5. Measured phase noise characteristics of a 500-MHz signal with spurs at an offset of 5 MHz generated due to the periodic substrate noise.



(a) (b)

Fig. 6. Location of the noise injector buffers (1, 2, 3) and the PLL. (a) Chip layout. (b) Die.

through their parasitic capacitance during signal transitions. The PLL blocks (the PFD, CP, VCO, divider, and LPF) and the decoupling capacitors have p^+ and n-well guard rings with the width of 20 μm around each [7]. All PLL blocks have localized the decoupling capacitors and a total on-chip decoupling capacitance of 1.5 nF. V_{DD} and ground (GND) connections each have five dedicated package pins to reduce the voltage drop over bondwire inductance ($\simeq$ 300 pH) [6]. External decoupling capacitors are also used to maintain the off-chip V_{DD} to the GND voltage constant. The substrate taps used in guard rings are connected to the circuit GND, such that the substrate noise picked up by the guard rings appear directly at the PLL GND node, as demonstrated in [9]. Fig. 6 shows the layout and die photo of the test chip, and the location of the noise injector buffers (1, 2, 3) and the PLL.

IV. Substrate Noise Versus Supply Noise Injection

The LPF (due to its large area) and the VCO are highly sensitive to substrate noise. The VCO is also sensitive to power supply noise, bondwire coupling, and other on-chip noise sources. Fig. 3 shows the on-chip test setup along with the parasitic components to the substrate to explain the phenomenon of coupling and to characterize the sensitivity of the PLL to substrate noise.

In Fig. 3, switches S_1-S_4 can be configured to explain the different modes of coupling to the VCO operating in an open loop with other PLL blocks in disabled mode and the clock signal given as the input to the noise injector buffers. The magnitude of the spurs in the output spectrum is monitored to characterize

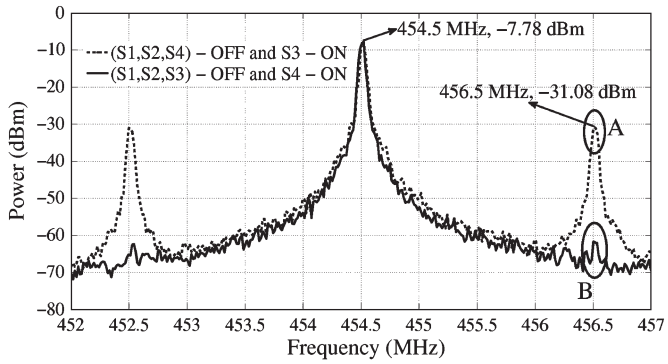


Fig. 7. VCO output spectrum (open loop) with spurs at an offset of 2 MHz in response to the 2-MHz noise injected into the substrate.

the sensitivity of the VCO to the injected noise. The spur level in the output spectrum is defined as

$$\text{Spur level, dBc} = 10 \cdot \log\left(\frac{P_{\text{spur}}}{P_{\text{carrier}}}\right) \quad (1)$$

where P_{spur} and P_{carrier} are the power at spur frequency and carrier frequency, respectively.

Case 1: S_1, S_2, and S_3 are OFF, and S_4 is ON. This enables the characterization of noise coupling directly to the VCO through the power supply, bondwires, or other modes. Fig. 7 shows the output spectrum of the VCO with spur B in response to a 2-MHz periodic signal given as the input to the noise injector buffers.

Case 2: S_1, S_2, and S_4 are OFF, and S_3 is ON. The LPF in the PLL is connected to the VCO, and the substrate noise picked up by the LPF is coupled to the VCO control voltage. The large spur A in the VCO output spectrum shown in Fig. 7 indicates that the primary mode of the noise coupling to the PLL is through the substrate noise picked up by the LPF.

Fig. 8(a) shows the sensitivity of the VCO gain (from the control voltage node to the VCO output) to the control voltage and W_p. Periodic noise of 10 MHz is injected into the substrate, with the test setup in Case 2 configuration, and the spur level in the VCO output at an offset of 10 MHz is monitored against VCO gain variations, keeping the noise source constant. Fig. 8(b) shows the sensitivity of the spur level of the VCO output to the control voltage. The spur characteristics measured by varying the control voltage are used to track the VCO gain variations. The analyses presented in Cases 1 and 2 confirm that the unwanted spurs in the VCO output spectrum are due to the periodic substrate noise picked up by the LPF coupled to the VCO control voltage and not through the supply voltage or bondwire coupling. Fig. 8 verifies this case.

The single-node bulk model proposed in [6] is used to simulate the test setup shown in Fig. 3. The p^+ bulk layer is represented by a single node. Resistors $R_{M1}-R_{M5}$ model the series resistance of the interconnect metal layers, and $R_{S1}-R_{S5}$ model the spreading resistance through the substrate. $C_{S1}-C_{S10}$ represent the capacitance between the interconnect lines and the substrate. C_{S11} models all capacitance between the bulk and the ac GND. Source and drain junction capacitance is included in the transistor model. $L_{b1}-L_{b8}$

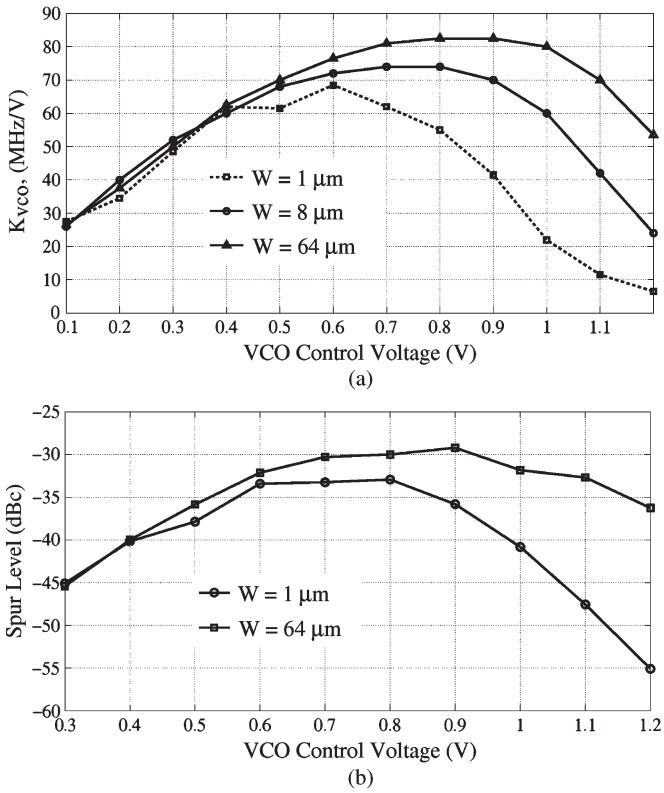


Fig. 8. Open-loop VCO characterization. (a) Sensitivity of the VCO gain to control voltage. (b) Spur-level dependence on the VCO control voltage.

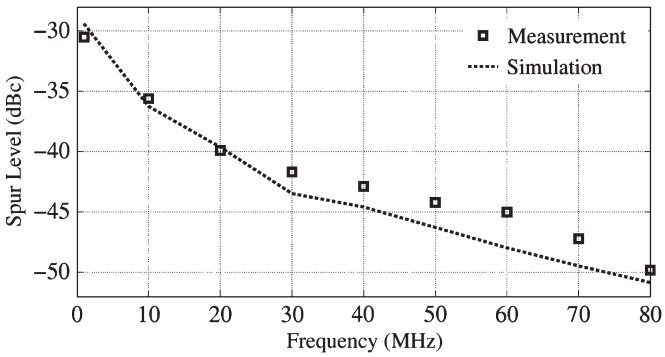


Fig. 9. Sensitivity of the VCO (open loop) output spur level to the periodic noise frequency.

represent the inductance associated with the bondwires. Resistance can be computed from the sheet resistance of the metal layers and the doping concentration of the substrate. Five dedicated package pins are used for the GND connection, accounting for a bondwire inductance L_{b8} of $\simeq$ 300 pH.

The amplitude response of the spur level depends on the strength of the noise injecting buffers, the interconnect capacitance to the substrate ($\simeq$ 200 fF), the inductance of bondwires, and the resistance from the bulk node to the ac GND ($\simeq 5\ \Omega$). The frequency response of the spur level largely depends on C_{S11} ($\simeq$ 95 pF) and the resistance from the bulk node to the ac ground. The other parasitic components have negligible effect on the spur characteristics. Fig. 9 shows the example correlation between the simulation and measured results of the spur level at the VCO output across different noise frequencies.

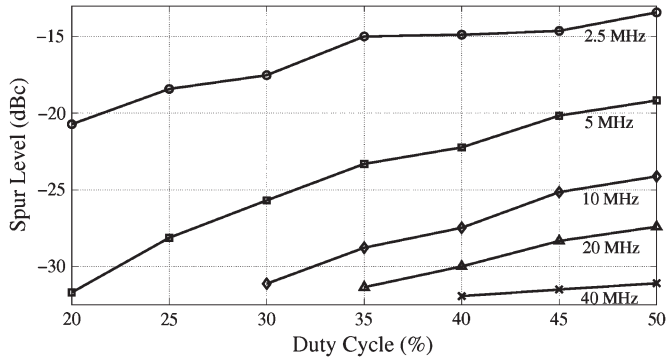


Fig. 10. Measured sensitivity of the PLL output spur level to the frequency and the duty cycle of the periodic substrate noise.

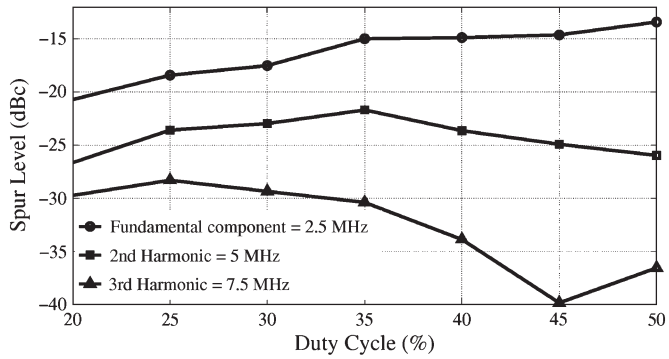


Fig. 11. Effect of the harmonic components of a pulsed clock on PLL output spurious tones.

V. Impact of a Pulsed Clocking Scheme on PLL Performance

In the given experiments, a conventional 50% duty-cycled clock signal is used for the substrate noise injection. Reducing the duty cycle of a clock signal reduces the power of its fundamental component (as shown in Fig. 2) and, hence, the injected substrate noise and its effect on the PLL performance. Fig. 10 shows the impact of the frequency and the duty cycle of the periodic substrate noise on the spur level at the PLL output.

The PLL exhibits low-pass characteristics to the substrate noise; thus, the spur level decreases upon reducing the duty cycle of the noise injector signal. The reduction in the spur levels by 3.36, 2.59, and 0.84 dB are observed at the offsets of 10, 20, and 40 MHz, respectively, upon reducing the duty cycle of the noise injector signal from 50% to 40%. The reduction in the spur level with the duty cycle at higher frequencies is low due to the low-pass filtering effect of the substrate.

The signal power at the fundamental frequency component decreases upon reducing the duty cycle, but the power level at other harmonics increase, as shown in Fig. 2. Hence, their corresponding output spur levels at the offset of the harmonic frequencies from the carrier also increase upon changing the duty cycle. Fig. 11 shows the effect of periodic substrate noise of 2.5 MHz and its harmonics on the corresponding spur levels at the PLL output. The spur-level characteristics at the harmonic frequency offsets, as a function of the duty cycle, follow the amplitude characteristics of the harmonic components of the clock signal shown in Fig. 2. The spur levels at higher harmonic

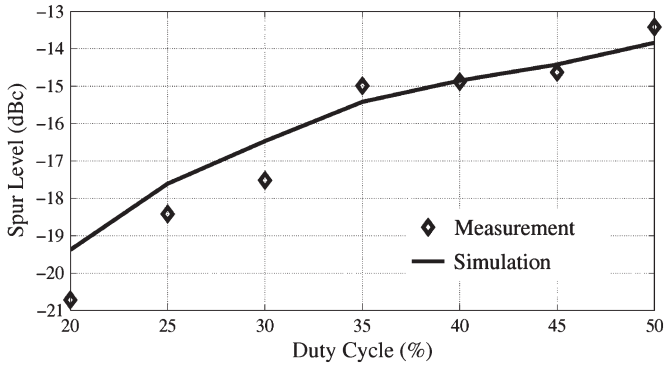


Fig. 12. Simulation and measured results of the sensitivity of the PLL output spur level to the duty cycle of the periodic substrate noise of 2.5 MHz.

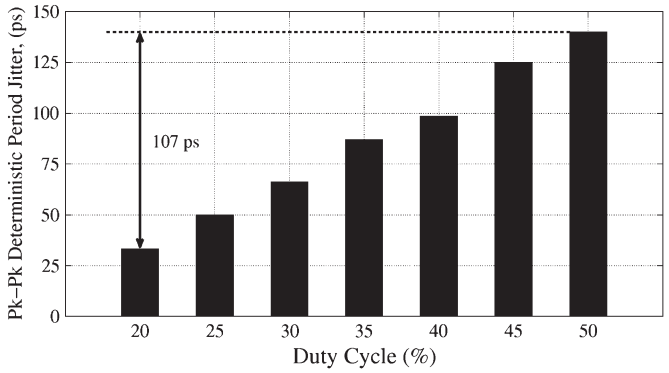


Fig. 13. Measured duty cycle effects of the 5-MHz noise injected into the substrate on the Pk–Pk deterministic period jitter.

frequency offsets are low due to their lower power content and the low-pass filtering effect of the substrate. Fig. 12 shows the correlation between the measured data and the simulation results of the PLL output spur-level dependence on the duty cycle, for the periodic noise of 2.5 MHz.

For the PLL output frequency of 500 MHz with periodic substrate noise of 5 MHz, a reduction of 12.53 dB in the output spur level and a reduction of 107 ps in the peak-to-peak (Pk–Pk) deterministic period jitter are observed upon reducing the duty cycle of the 5-MHz pulsed clock from 50% to 20%. Fig. 13 shows the duty cycle effects of the substrate noise of 5 MHz on the Pk–Pk deterministic period jitter of a 500-MHz carrier signal.

VI. Conclusion

The effects of the periodic substrate noise generated from pulsed clock buffers on the output spur level, the Pk–Pk deterministic period jitter, and the phase noise of PLL performance metrics have been demonstrated experimentally. The phenomenon of substrate noise coupling to the PLL via the LPF has been also explained through the experiments. Upon decreasing the duty cycle of the noise injector signal from 50% to 20%, a reduction of 12.53 dB in the spur level at an offset of 5 MHz from a 500-MHz carrier and a reduction of 107 ps in the Pk–Pk deterministic period jitter have been observed. The results of the analyses suggest that the operation of digital systems with a pulsed clocking scheme along with conventional substrate noise reduction techniques helps in the efficient integration of sensitive analog/RF circuits with noisy digital systems, achieving enhanced functionality on a single chip.

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