Tutorial on Mixed mode simulation and simulation of spice netlists in Cadence

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This tutorial will show you how to simulate a mixed-mode circuit, a circuit partly described by verilog and partly by circuit elements such as resistors, capacitors, transistors etc. in Cadence IC5141. It will also show you how to directly simulate a SPICE netlist without having to create schematic and symbol views in Cadence. The demonstration is made by building a window comparator using two discrete op-amps (described by a manufacturer provided SPICE macro-model) and an AND gate(described by verilog).

1 Introudction

Manufacturers of discrete components such as off-the-shelf op-amps typically provide SPICE macro models. However, symbol/schematic views for such parts are rarely available (schematic view is usually not available for standard cells either). One way to go about simulating a circuit with such off-the-shelf op-amps is to read in the SPICE netlist provided by the manufacturer and create a schematic and symbol view for them. This tends to be a laborious and error-prone process since SPICE streamin is an unsupported feature in Cadence IC5141. A simpler approach is to simulate the netlist directly, without creating schematic or symbol views[2]. In this tutorial, we'll build and simulate a window comparator shown in Fig. 1. The model of the opamps is obtained from the manufacturer[3] and in a spice netlist, we'll connect the op-amps as shown in Fig. 1 to complete the analog section of the circuit. Verilog is written for the digital section. The two sections are connected together in Cadence schematic editor and SpectreVerilog is used for simulation[1]. To get started, fire up Cadence and create a new library (say "mixedtutorial") attached to UMC13MMRF.

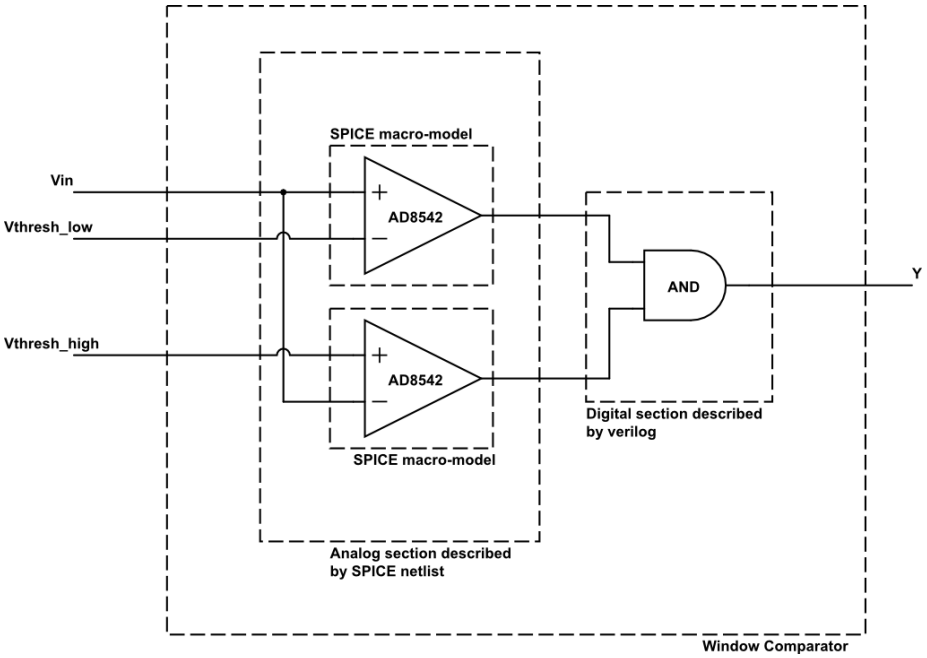

Figure 1: Window Comparator

2 The digital section

In the library mixedtutorial, create a new cell-view "andgate" with "functional" as the View name and "Verilog-editor" as the tool (see Fig. 2). When you click on OK, a text editor should open up. Write code for the AND gate as shown in Fig. 3. Hit ESC and :wq to save and quit the editor. You may ignore warnings for now. When asked if you want to create a symbol view, hit yes. And voila ! You're done with the digital section.

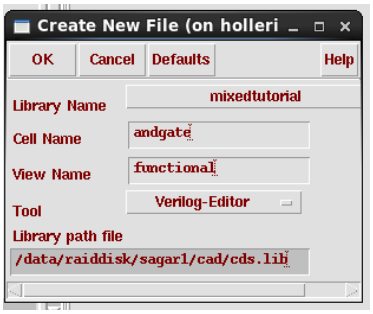

Figure 2: Creating a verilog cell-view

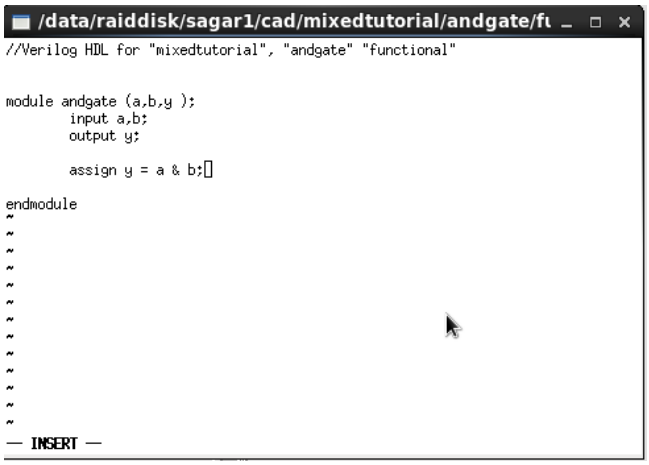

Figure 3: Verilog view for AND gate

3 The analog section

Download the spice macromodel for AD8542 from [2] and save it to "AD8542.spi" (I put it in /data/raiddisk/sagar1/cad/mixedtutorial/code/AD8542.spi). We'll name the analog section of the circuit in Fig. 1 as "analogwindow". The "analogwindow" subcircuit will have these ports(7 in number): AVDD, AGND, VThreshlow, VThreshhigh, Vin, O1, O2. Because Cadence likes to insert an extra reference port when spice netlists are invoked from the schematic editor, we'll place another port which we shall call "dummy" and never use it (This is only necessary for the top subckt in the spice netlist that you want to expose to the Cadence schematic editor). Now, write the contents of Listing 1 to a file (I put it in /data/raiddisk/sagar1/cad/mixedtutorial/code/analogwindow.spi). The analog section is done.

Listing 1: analogwindow.spi

```
*First line in SPICE is always a comment !

.include /data/raiddisk/sagar1/cad/mixedtutorial/code/AD8542.spi

.SUBCKT analogwindow AVDD AGND VThreshlow VThreshhigh Vin O1 O2 dummy

X1 Vin VThreshlow AVDD AGND O1 AD8542
X2 VThreshhigh Vin AVDD AGND O2 AD8542

.ENDS analogwindow
```

4 Putting them together

Create a new schematic cell-view "windowcomparator" in the library "mixedtutorial". Insert a component "scasubckt" from analogLib to instantiate the spice netlist we created (see Fig. 4). When counting the number of ports, do NOT

include "dummy" in the count. Instantiate the AND gate created with verilog in the usual way and make connections. The final schematic which includes the test voltage sources is shown in Fig. 5. Every digital IO pin has to be connected to something "analog" for the mixed mode simulation to work right. To do this, add 1fF caps to all digital lines.

Figure 4: Instantiating a SPICE netlist in the schematic

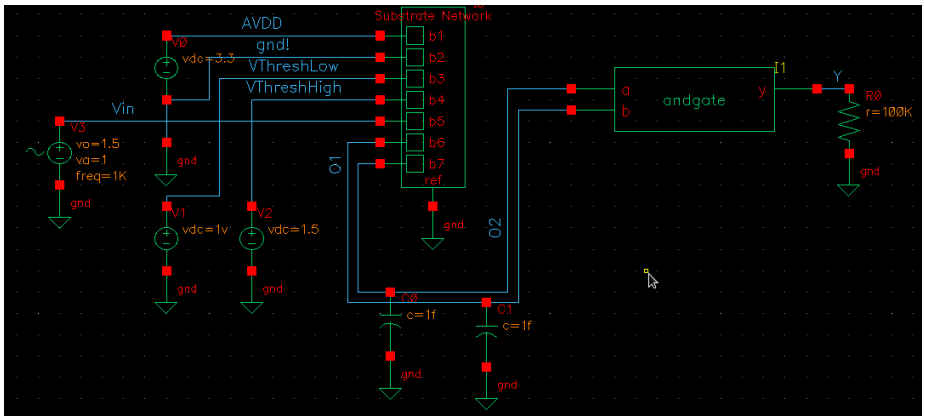

Figure 5: Completed window comparator schematic with test voltage sources

Now, close the schematic and create a "config" view with "Hierarchy-editor" tool for the same cell (the one with the schematic you just made including the SPICE netlist and AND gate instantiated. In my case, it is "windowcompara-

tor") as shown in Fig. 6.

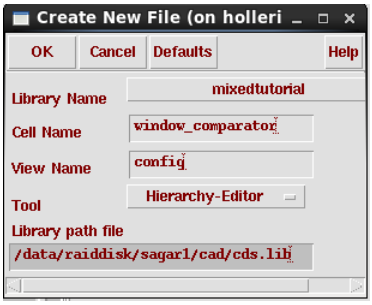

Figure 6: Config view for the mixed mode schematic

Click on "Browse" and select the schematic view of your mixed mode circuit in the library browser as shown in Fig. 7.

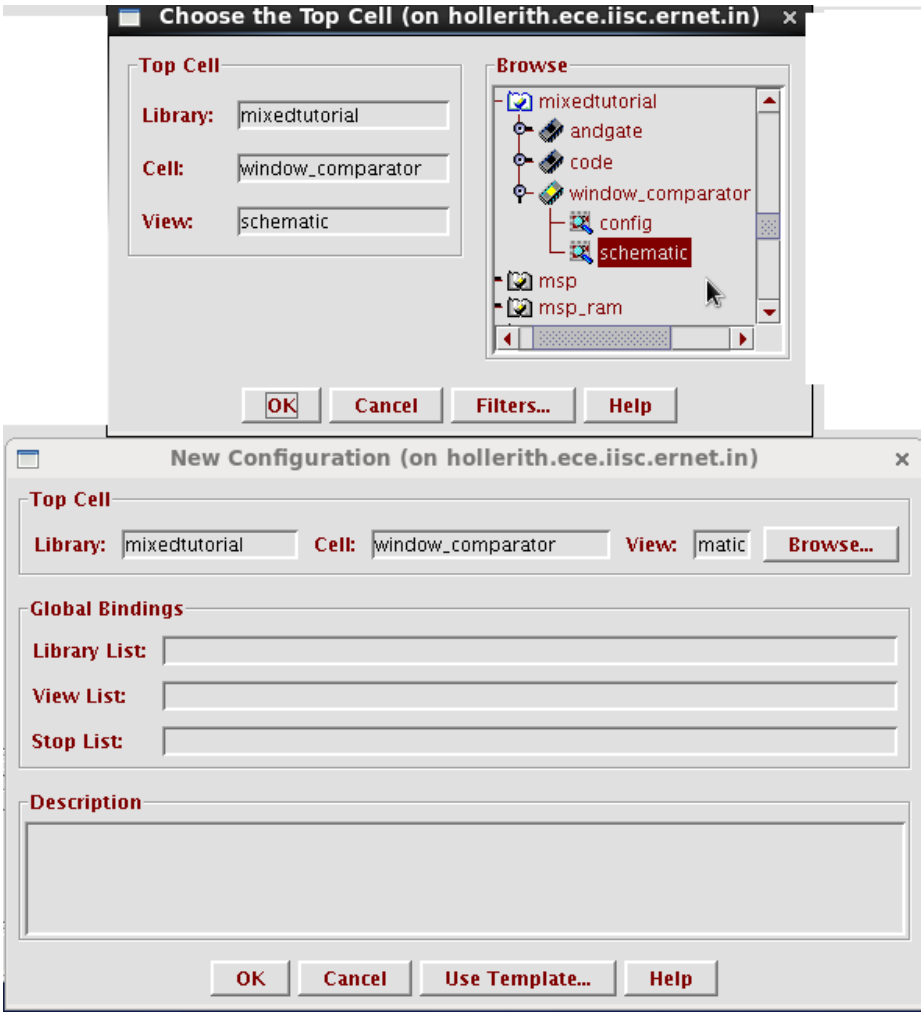

Figure 7: Browse to select the mixed mode schematic

Now, click on "Use Template". Choose "SpectreVerilog" from the list and Click OK. In the "LibraryList" field, enter "mixedtutorial" which is the library you are using for this tutorial. Finally, the new config dialog box should look similar to Fig. 8.

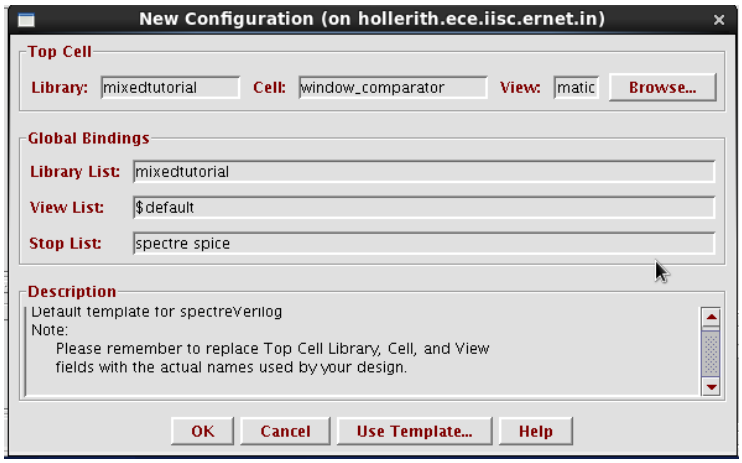

Figure 8: New Configuration Dialog box after setting everything

In the hierarchy-editor, click View -⟩ Update and then File -⟩ Save and close the hierarchy editor.

Open the "config" view and click on "yes" to both for edit mode. Goto Tools, Analog Environment to start the simulation. Click Setup, Simulator and choose "SpectreVerilog" as the simulator and select the desired nets (Vin and Y) for plotting. You'll probably find that the AND gate is not working. This is because the logic thresholds which convert analog voltages to digital values and vice versa are by default set to 5v logic. This can be changed by going to the newly opened schematic editor, Mixed Signal, Interface elements, Library. You can also change the rise time and fall time of digital signals being connected to analog components here.

5 Simulation results

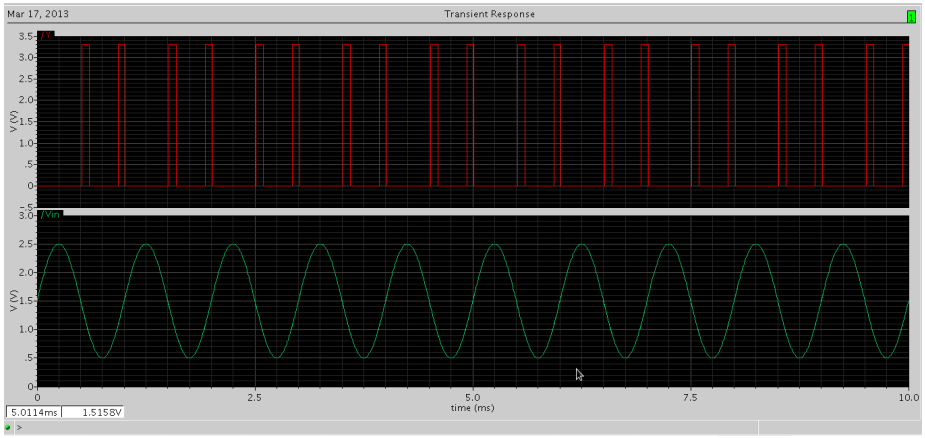

Figure 9: Window comparator detects when Vin is between 1 and 1.5v

6 Conclusion

This tutorial demonstrated the simulation of a mixed signal circuit. Simulating a SPICE netlist directly without creating schematic/symbol views was shown. This is particularly useful when simulating SPICE macro models of off-the-shelf components and standard cells for which schematic/symbol view is unavailable.

References

[1] J.Wade, Cadence Mixed Signal Tutorial, `http://bit.ly/YhkSmd`

[2] T.Wilsey, How to Simulate a Subcircuit in Spectre, `http://bit.ly/p1HxaW`

[3] Spice Macro-model for AD8542, `http://bit.ly/Xho4ux`