Within-Die Gate Delay Variability Measurement using Re-configurable Ring Oscillator

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***Abstract*—We report a circuit technique to measure the on-chip delay of an individual logic gate (both inverting and non-inverting) in its unmodified form using digitally reconfigurable ring oscillator (RO). Solving a system of linear equations with different configuration setting of the RO gives delay of an individual gate. Experimental results from a test chip in 65nm process node show the feasibility of measuring the delay of an individual inverter to within 1pS accuracy. Delay measurements of different nominally identical inverters in close physical proximity show variations of up to 26% indicating the large impact of local or within-die variations.**

I. Introduction

A typical design today involves a high level of integration along with high data transmission rate in the order of gigabytes per second which necessitates a much more accurate timing analysis of digital system. Timing analysis using corner models lead to over-design. Instead, statistical models are being developed to give realistic picture of timing analysis. To validate statistical models, we need test circuit to measure the process variation effects [1]. In advanced process nodes, other effects like poly-pitch effect, stress effect and neighborhood effect need accurate characterization. These requirements motivated us to develop techniques to measure delay of the individual standard cells inside the chip.

The source of process variations can be divided into the following two categories: 1) inter-die or global or die-to-die variations; and 2) intra-die or local or within-die variations.

In the recent past, attempts were made by several researchers [2] [3] towards the measurement of random local variability. Besides measuring the device parameters like threshold voltage, oxide thickness, length etc, we would like to directly measure the delay of individual standard cells, as that is the parameter of interest in the statistical timing analysis tool.

Picosecond Imaging Circuit Analysis (PICA) [4] is used to obtain quantitative delay information by counting the number of infra-red photons from the back side of a thinned package chip. However, the technique requires infra-red measurement which makes it costly and tedious. Delay measurement based on Delay Lock Loop(DLL) was proposed by [5]. Even this solution looks promising in measuring to sub-nanosecond resolution of the cells under test. However, the complexity of the on-chip measurement circuitry limits its large scale implementation which will be needed for characterizing variations. The authors in [6] proposed random sampling technique to measure the delay of standard cells. In this technique, two samplers are used to sample the input and output of the cell. Due to local process variation [7], the two samplers will suffer from variation and hence the measurement will be inaccurate.

Normally, the delay of a cell is quite small; delay can be amplified by cascading a number of stages and the delay of the individual cell can be found out by averaging. Traditional way of measurement of propagation delay variation due to process variations is usually performed with ring oscillator (RO) because of its easy on-chip implementation and high sensitivity to process parameter [8] [9] [10] [11]. However, it is difficult to extract gate to gate delay variation from a simple ring oscillator. It might be possible to use very small rings 3-5 stages, but the frequency will be very high leading to complexity in implementation.

Authors in [12] have presented a technique to measure incremental delay i.e. the difference between the two propagation delays of the same cell. In this technique, the authors have modified the cell and formed ring oscillator using these cells. The main drawback of this approach is that the modified cells are not a cell of any standard cell library. Hence, this approach is not suitable for delay mismatch measurement of standard cell library.

A method to measure cell-to-cell delay mismatch due to process variations is presented in [13]. In this approach, the cell is a combination of inverter and transmission gate. The authors in [13], point out the importance of the symmetry in the ring oscillator based measurement technique. However, the layout of the structure is not regular because of multiplexer used outside the ring.

Our contribution in this work is in-situ measurement of standard cell gate delay (both inverting and non-inverting) in its unmodified form. The proposed approach is also useful in measuring delay variation due to local transistor variability, neighborhood effects, voltage and temperature variations.

II. Gate Delay Measurement Cell

Fig. 1 shows the basic concept of delay measurement technique. There are two paths between input to output. The difference of delay between two paths conceptually gives the delay of the gate under test. Fig. 2 shows schematic of proposed gate delay measurement cell (GDMC). This cell consists of two different types of inverters and two multiplexers. The inverter I_1 is the gate whose delay is to be measured. The

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inverters I_2, I_3, I_4 and I_5 are used for buffering and load matching. The multiplexer Mux_1 allows bypassing of the logic gate, thus enabling the calculation of the gate's delay by the difference of two period measurements of the ring oscillator. Thus, the calculated delay will be the sum of the delay of the logic gate and the difference in path delays of the multiplexer Mux_1 (i.e between input A to output Y and input B to output Y) due to unequal slew input to two inputs of Mux_1 for the two different mux settings.

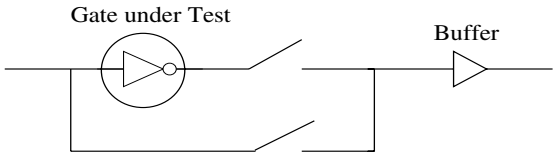


Fig. 1. Concept of gate delay measurement

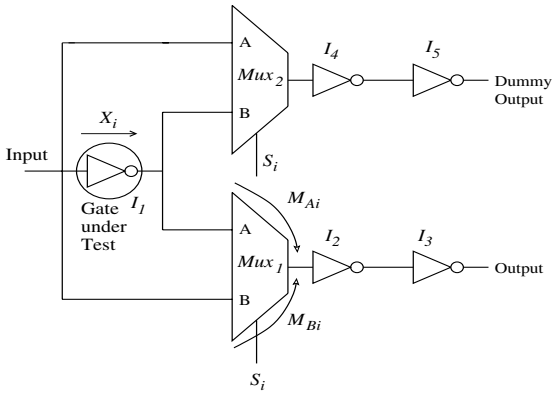


Fig. 2. Schematic of a Gate Delay Measurement Cell

The input signal to the stage is connected both directly and through inverter I_1, to the two inputs of the multiplexer Mux_1. The output Y of the multiplexer is driven out through inverters I_2 and I_3 which buffers the cell from configuration changes in the subsequent stage. Multiplexer Mux_2 and inverters I_4, I_5 are a dummy structure used to provide equal loading to inverter I_3 of the previous stage irrespective of status of the select input of the multiplexers. Symmetric multiplexers of large size which have balanced delays between input A to output Y and input B to output Y are used to reduce any systematic mismatches. The sizes of multiplexer Mux_1, inverters I_2, I_3 are same as of multiplexer Mux_2, inverters I_4, I_5 respectively. The multiplexer Mux_1 and Mux_2 are matched in the layout.

The above structure allows symmetry and load matching which helps in finding the individual gate delay. In the absence of process variation all the T-stage delays (i.e. T=any odd number $\leq N$ where N is number of stages in RO) in ring oscillators should produce equal delays. In the absence of process variation, the delay of inverter I_2 and I_3 should be same irrespective of the status of the control inputs.

III. Reconfigurable Ring Oscillator Structure

For simplicity of description, we have considered a 5-stage ring oscillator below. However, the technique is applicable for any number of stages of ring oscillator. With this circuit setup, it is shown that delay of inverting gate can be measured using this structure.

A. Inverting gate delay measurement

Fig. 3 shows the delay measurement circuit for inverting gate. The technique of delay measurement for inverting gate is presented below. Here X_i is the average of rise and fall delay of the i^{th} inverter I_1 under test, and M_{Ai} and M_{Bi} are the delays between inputs A and B to output Y of the multiplexer Mux_1. K is the delay of the rest of the elements of the ring oscillator like the buffers consisting of inverters I_2, I_3 of all the cells, the wires etc. I_4, I_5 will not contribute to the frequency of the RO, because it is not part of the ring. Note all the delays are average of rise and fall delays. Let S be the configuration vector consisting of 5 bits. If S_i = 0, then input A to output Y of the multiplexer Mux_1 of the i^{th} stage GDMC is selected. If S_i = 1, then input B to output Y of the multiplexer Mux_1 of the i^{th} stage GDMC is selected. T_1, T_2, T_3 and T_4 are the period of RO for four configuration vectors S = 00000, 00011, 00110, 00101 respectively. The delay measurement of inverting gate requires four configuration vectors or control words. Since, each GDMC switches twice during a complete cycle, the sum of all the average cell delays equates to half a clock period of the RO signal.

When select status vector S = 00000, then the input A to output Y of stages 1st, 2nd, 3rd, 4th, 5th are connected. Then,

$$\sum_{i=1}^{5}(X_i + M_{Ai}) + K = T_1/2 \tag{1}$$

When select status vector S = 00011, then the input A to output Y of stages 1st, 2nd, 3rd are connected and the input B to output Y of stages 4th and 5th are connected.

$$\sum_{i=1}^{3}(X_i + M_{Ai}) + \sum_{i=4}^{5} M_{Bi} + K = T_2/2 \tag{2}$$

Taking the difference between Eq. (1) and (2), we get

$$X_4 + M_{A4} + X_5 + M_{A5} - M_{B4} - M_{B5} = (T_1 - T_2)/2 \tag{3}$$

When select status vector S = 00110, then the input A to output Y of stages 1st, 2nd, 5rd are connected and the input B to output Y of stages 3th and 4th are connected.

$$\sum_{i=1,2,5}(X_i + M_{Ai}) + \sum_{i=3}^{4} M_{Bi} + K = T_3/2 \tag{4}$$

When select status vector S = 00101, then the input A to output Y of stages 1st, 2nd, 4th are connected and the input B to output Y of stages 3rd and 5th are connected.

$$\sum_{i=1,2,4}(X_i + M_{Ai}) + \sum_{i=3,5} M_{Bi} + K = T_4/2 \tag{5}$$

Taking the difference between Eq. (4) and (5), we get

$$-X_4 - M_{A4} + X_5 + M_{A5} + M_{B4} - M_{B5} = (T_3 - T_4)/2 \quad (6)$$

Adding the Equations (3) and (6), we get

$$X_5 + (M_{A5} - M_{B5}) = (T_1 - T_2 + T_3 - T_4)/4 \quad (7)$$

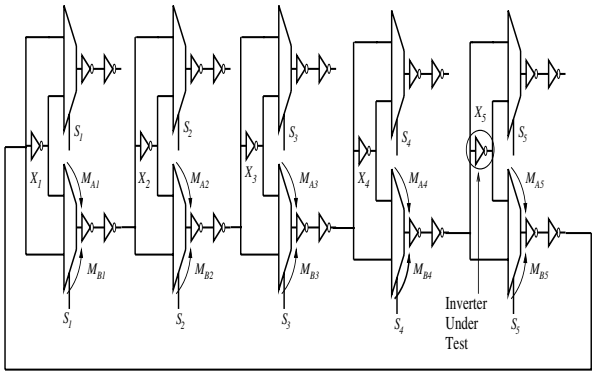


Fig. 3. Inverting Gate Delay Measurement showing Inverter under test

Period measurements of the ring oscillator T_1-T_4, with four different control word settings lead to the Eq. 7 for the delay of inverter I_1 in the 5th stage along with the residual error term, which is the difference between input A to output Y and input B to output Y delays of the multiplexer Mux_1. However, unequal slew rate at the two inputs of Mux_1 for the two different mux settings contributes to a residual delay error between the A, B inputs and mux output, which is observed to be 1.2pS from circuit simulations of extracted layout in the absence of process variation. Since the proposed technique requires the computation of difference of linear equation, the residual error term for the mux delay mismatch cancels out the global transistor variation component term leaving behind the local variation term. However, X_5 includes nominal delay plus global and local variation terms.

The minimum number of stages required for this type of delay measurement is four or five for non-inverting or inverting gate delay measurement respectively. Since odd number of stage ROs can be formed, the number of equations formed using 5-stage RO are $C(5,5)$ + $C(5,3)$ = 11 and number of variables (e.g. gate delays to be measured) is 5. Hence the delays can be cross checked across many different measurements similar to [12]. For our test chip, measurements of 22 different gates each with 6 different configurations yields the delay values for the corresponding gates to be within 0.64pS (refer to Fig.7(b)), indicating the robustness of the measurements.

The technique presented here shows the on-chip measurement of inverter. However, if we replace inverter I_1 of Fig. 2 with any inverting gate, then delay of that gate can be measured. Similarly, the delay of non-inverting gate can also be measured with only two configuration vectors or control words.

IV. Chip Results

The layout of the test chip with the distribution of ring oscillators is shown in Fig. 4. The divider is used to slow down the frequency because the I/O has a frequency limitation of 100MHz. Each gate's delay measurement requires period measurements for four different oscillator configurations for inverting gate as described in Eq. 7.

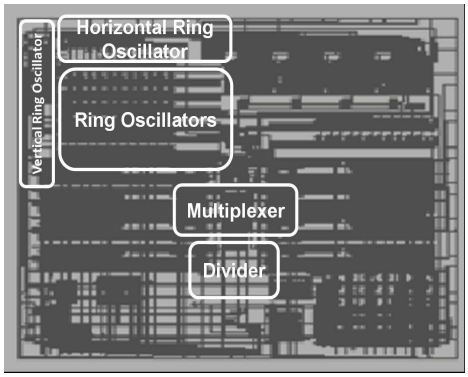


Fig. 4. Layout of test chip showing the distribution of ring oscillators

Fig. 5 shows the measured individual delays of inverter I_1 (refer to Fig. 2) (normalized to a fan-out 1 loaded inverter) in each of the 10 stages of the same ring from two different chips. The inverter to inverter delay in the ring, as a percentage of the mean delay varies by up to 26% for chip 1 and 17.4% for chip 2, indicating the effect of intra-chip local variations. There is no discernible pattern of variation for the delays within the same ring. Between the two chips, the variation pattern has some similarity, for stages 4 to 8, but is different for the rest indicating the randomness of these local or within-die variations.

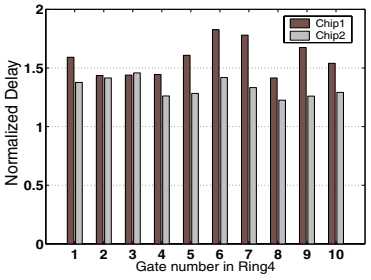
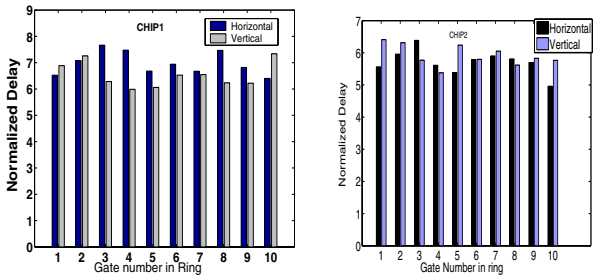


Fig. 5. Measured delays of 10 nominally identical inverters in the same ring from different chips

We also correlated the measured results to results from statistical SPICE simulation and found that out of 20 measured delays from two chips (see Fig. 5), 17 points were well within the distribution whereas the rest of the points lie towards the tail of the distribution.

We apply this gate delay measurement to study the delay variation due to orientation in layout. Fig. 6(a) shows the delays of the 10 inverters in two ring oscillators, one laid out vertically and the other horizontally for chip1, showing a

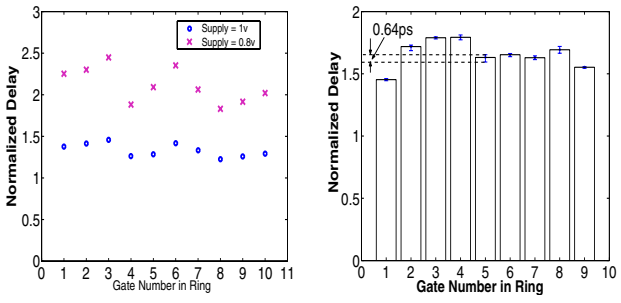
delay spread of 19%. Note that in these two rings, the inverter I_1 has a different size, layout and loading compared to that of Fig. 5. The pattern of local delay variation is different for the vertical and horizontal cells. Fig. 6(b) shows the delays of the 10 identical inverters in horizontal and vertical ring oscillators for chip2. Comparison of Fig. 6(a) and Fig. 6(b) shows the gate number 1,2,3,4,8 and 10 have a pattern of similarity where rest of the gates show opposite pattern signifying the importance of random variation.



(a) Chip1 (b) Chip2

Fig. 6. Measured delays of 10 nominally identical inverters in horizontal and vertical orientation of RO

Fig. 7(a) shows the measured delay variations of the 10 cells in a ring for two different supply voltages. We observe that the delay and the delay spread at 0.8V are more than for 1V, but the pattern of variation is the same. As we decrease the supply voltage, the spread in delays increases from 17% at 1V to 29% at 0.8V, indicating that the main source of local variations is the process.



(a) (b)

Fig. 7. (a) Measured gate delays in a ring for 1V and 0.8V supply (b) Error in Delay measurement of different gates

The error in delay measurement is shown in Fig.7(b). As mentioned earlier, same gate delay can be measured in multiple ways, because the number of equation is more than the number of variables. Here the number of equation means the different RO oscillator configuration setting and the number of variables is the number of gate delay to be measured. Fig.7(b) shows 9 different gates, each gate delay is measured in 6 different ways. The maximum error in delay measurement in Fig.7(b) is found to be 0.64ps. This proves the robustness of delay measurement to be within 1pS accuracy.

These measurements indicate that local gate to gate variations are very significant in advanced process nodes and need to be accounted in the models and design practices. The presented measurement technique is simple yet powerful to study these variations.

V. Conclusion

A circuit technique has been developed to measure the delay of individual gates using reconfigurable ring oscillators in standard cell library inside the chip. The technique is all-digital in nature and can be easily embedded within standard digital logic to perform in-situ measurement. The results from 65nm test chip show the efficacy of measurement to within 1pS accuracy. Delay measurements of different nominally identical inverters in close physical proximity shows variations of up to 26% indicating the large impact of local variations. The proposed technique is quite suitable for early process characterization, monitoring mature process in manufacturing, correlating model-to-hardware and study local variation and neighborhood effects.

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