VLSI Interconnect - II
Interconnect Sketch in 3D

[Picture from http://www.mit.edu/~yuchsiao/caplet/img/home.png]
Simple RC model

\[ R = \frac{\rho L}{WH} \]

\[ C_{ox} = K_{ox} \varepsilon_o \frac{WL}{X_{ox}} \]

\[ C_I = K_{ox} \varepsilon_o \frac{HL}{L_S} \]
Resistance per square concept

Sheet resistance

\[ R = \frac{\rho}{t/w} \]

Depends on thickness and hence Layer number

100mohm to 1mohm per square
2-20ohms per via. So don’t forget them!
Put as many as possible to reduce their impact.
Lumped model of a long wire

Up to 3 segments of PI model are sufficient to model the delay and slew at receiver.
Example: 1

1mm wire with 100mohms/um and 0.2fF/um

R_{wire} = 100\,\text{ohms}, \quad C_{wire} = 0.2\,\text{pF}

Use 3-segment pi model. Each resistance = 100/3 ohms and each capacitance is 0.2pF/6
Example 3

\[ T_{D_3} = R_1 C_1 + (R_1 + R_2) C_2 + (R_1 + R_2 + R_3) C_3 + R_1 C_4 \]
\[ T_{D_4} = R_1 C_1 + R_1 (C_2 + C_3) + (R_1 + R_4) C_4 \]
Repeaters

(a)

Wire Length: \( l \)

Driver

Receiver

N Segments

Segment

Driver

Repeater

Repeater

Repeater

Repeater

Receiver

(b)
Optimal repeater insertion to minimize delay

Given:
\[ R_w = \text{Wire resistance per unit length} \]
\[ C_w = \text{Wire capacitance per unit length} \]
\[ R_g = \text{Inverter resistance per unit size} \]
\[ C_g = \text{Inverter input capacitance per unit size} \]
\[ C_d = \text{Inverter output capacitance per unit size} \]

To be obtained:
\[ S = \text{Size of each inverter} \]
\[ N = \text{Number of inverters} \]
Single Stage Delay

\[ D_i = \frac{R_g}{S} * ((C_d + C_g) * S + \frac{C_w * L}{N}) + R_w \frac{L}{N} * (\frac{C_w}{2} \frac{L}{N} + C_g * S) \]

\[ D_i = R_g (C_d + C_g) + \frac{R_w C_w L^2}{2N^2} + \frac{R_g C_w L}{SN} + \frac{R_w L C_g S}{N} \]

\[ D = N D_i = R_g (C_d + C_g) * N + \frac{R_w C_w L^2}{2N} + \frac{R_g C_w L}{S} + R_w L C_g S \]
Minimize delay

\[ D = R_g (C_d + C_g) N + \frac{R_w C_w L^2}{2N} + \frac{R_g C_w L}{S} + R_w L C_g S \]

\[ \frac{\partial D}{\partial S} = 0 \Rightarrow R_w L C_g * S_{opt} = \frac{R_g C_w L}{S_{opt}} \]

\[ S_{opt} = \sqrt{\frac{R_g / C_g}{R_w / C_w}} \]

\[ D_{opt} = L \times 2 \times (\sqrt{0.5 R_g (C_d + C_g) R_w C_w} + \sqrt{R_g C_g R_w C_w}) \]

\[ \frac{D_{opt}}{L} = \sqrt{\frac{R_g C_g}{R_w C_w}} \sqrt{R_w C_w} \times (2 + \sqrt{2 \left(1 + \frac{C_d}{C_g}\right)}) \approx 1.67 \sqrt{FO4 R_w C_w} \]

\[ \frac{L}{N_{opt}} = \frac{\sqrt{R_g C_g}}{\sqrt{R_w C_w}} \times 2 \left(1 + \frac{C_d}{C_g}\right) \]
Some Numbers

- ITRS documents
- Scaling
- 20nm process (2016), $R_w=96\text{k}\Omega/\text{mm}$, $c_w=0.2\text{pF/}\text{mm}$
  
  - FO4 $\sim 20/3 = 6.67\text{pS}$
  
  - Delay/mm $= 1.67 \sqrt{15\text{ps} \times 96\text{k} \times 0.2\text{pF}} = 597\text{pS}$
  
  - Delay without repeater/mm $= 0.5 \times 96\text{k} \times 0.2\text{pF} = 17.2\text{nS}$!
  
  - No of FO4 delays per mm of wire: $597/6.7 \sim 90$!
  
  - Speed of light delay: $6\text{pS/mm}$!

- Reducing the long-wire delay
  
  - Use global wires
  
  - Use wider wires and larger pitch
## Cross talk

![Cross talk schematic](image)

<table>
<thead>
<tr>
<th>B</th>
<th>$C_{\text{eff}}(A)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant</td>
<td>$C_{\text{gnd}} + C_{\text{adj}}$</td>
</tr>
<tr>
<td>Same as A</td>
<td>$C_{\text{gnd}}$</td>
</tr>
<tr>
<td>Opposite to A</td>
<td>$C_{\text{gnd}} + 2C_{\text{adj}}$</td>
</tr>
</tbody>
</table>
Noise coupling

\[ \Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gnd-v}} + C_{\text{adj}}} \Delta V_{\text{aggressor}} \]
Noise coupling with driver impedance

\[ \Delta V_{\text{victim}} = \frac{C_{\text{adj}}}{C_{\text{gndv}} + C_{\text{adj}}} \frac{1}{1+k} \Delta V_{\text{aggressor}} \]

\[ k = \frac{\tau_{\text{aggressor}}}{\tau_{\text{victim}}} = \frac{R_{\text{aggressor}}}{R_{\text{victim}}} \left( \frac{C_{\text{gnda}} + C_{\text{adj}}}{C_{\text{gndv}} + C_{\text{adj}}} \right) \]
Reducing cross talk

Shielding with power/gnd

Interleaving with other signals intelligently
Twisting and staggering

Figure 4.56 Crosstalk control schemes