Introduction to SRAM

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Memory Categories

- **Random Access Memory**
  - **Volatile Memory (RAM)**
    - Static RAM (SRAM)
    - Dynamic RAM (DRAM)
  - **Nonvolatile Memory (ROM)**
    - Mask ROM
    - Programmable ROM (PROM)
    - Erasable Programmable ROM (EPROM)
- **Serial Access Memory**
  - **Shift Registers**
    - Serial In Parallel Out (SIPO)
    - Parallel In Serial Out (PISO)
  - **Content Addressable Memory (CAM)**
    - First In First Out (FIFO)
    - Last In First Out (LIFO)
- **Queues**
  - Flash ROM
Static Memory Element
Flip Flop

Edge Triggered: So can chain them easily to form shift registers
Serial In Serial Out

Diagram showing a serial in serial out circuit with FF0, FF1, FF2, and FF3 registers.
Serial in Parallel Out
Enabled Flop
Serial In Parallel Out with Load Enable
Watch out for Hold Violations
Fixing hold violations

Delay is added
Use of Flop versus Latch

• Latch has lower area and power
• Hold violations are much more difficult to deal with in a latch based design
• However where hold violations are not an issue, use a latch over a flop to save area
Parallel In Serial Out
Random Access Memory

![Diagram of Random Access Memory](image_url)
Row Decoder
Improving the row decoder
A 16 entry LUT
SRAM Cell

Only 6 transistors: A latch with output mux has 12 transistors
Read Operation

(a) Circuit diagram showing components labeled as bit, bit_b, word, P1, P2, and D1, D2.

(b) Graph showing waveforms for Q, Q_b, bit, and bit_b over time (t), with labels for word and Q.
Write Operation

[Diagram of a circuit with labels: bit, bit_b, word, A_1, A_2, P_1, P_2, Q, D_1, D_2, Q_b, bit_b, word, Q, Q_b]
Read Circuitry

Bitline Conditioning

More Cells

word_q1

SRAM Cell

out_b_v1r

out_v1r

bit_v1f
Write Circuitry

Bitline Conditioning

More Cells

SRAM Cell

Write Driver

word_q1

data_s1