Test Power Case Study:
Transition Fault Testing (LOC, LOS) Power Analysis and Reduction Techniques

Based on the paper
pp.403-408  (Authors: Agarwal, K. et al)
Outline

• Trends in TFT Power Consumption

• LOC vs LOS: Detailed Power Comparisons and Analysis

• Reduction Techniques
Trends in TFT Power Consumption

Fmax plot for a 90nm SOC (silicon data)

Results from IR drop analysis

<table>
<thead>
<tr>
<th>Test</th>
<th>Module1</th>
<th>Module2</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOS</td>
<td>1.05</td>
<td>1.21</td>
</tr>
<tr>
<td>LOC</td>
<td>0.779</td>
<td>0.475</td>
</tr>
</tbody>
</table>

Max power consumption (W)

Test Module1 Module2

LOC 0.779 0.475

Fmax frequency difference suspected to be due to high switching activity in LoS

Devices ordered based on LOS Fmax frequency

1 175 349 523 697 871 1045 1219 1393 1567 1741 1915 2089 2263 2437 2611 2785 2959 3133
LOS Vs. LOC Capture Power Comparison

• LOC vs. LOS power comparison done on two example designs
  – Ckt1a : with clock gates
  – Ckt2a : without clock gates
  – Ckt1b : compression inserted Ckt1a
  – Ckt2b : compression inserted Ckt2a
## Most Power Consuming Pattern Comparisons

<table>
<thead>
<tr>
<th></th>
<th>LOC launch (mW)</th>
<th>LOC capture (mW)</th>
<th>LOS launch (mW)</th>
<th>LOS capture (mW)</th>
<th>LOS launch Vs LOC launch</th>
<th>LOS capture Vs LOC launch</th>
<th>LOS capture Vs LOC launch</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ckt1a</td>
<td>683</td>
<td>520.5</td>
<td>1137</td>
<td>667</td>
<td>66.47%</td>
<td>28.14%</td>
<td>-0.02%</td>
</tr>
<tr>
<td>Ckt2a</td>
<td>1025</td>
<td>958</td>
<td>1165</td>
<td>918</td>
<td>13.65%</td>
<td>-0.04%</td>
<td>-0.1%</td>
</tr>
<tr>
<td>Ckt1b</td>
<td>524</td>
<td>371</td>
<td>1025</td>
<td>551</td>
<td>95.6%</td>
<td>48.5%</td>
<td>0.05%</td>
</tr>
<tr>
<td>Ckt2b</td>
<td>870</td>
<td>748</td>
<td>1028</td>
<td>857</td>
<td>18.16%</td>
<td>14.57%</td>
<td>-0.01%</td>
</tr>
</tbody>
</table>

- LOS Launch > LOC Launch
- LOS capture ~ LOC Launch
- The difference between LOS launch power and LOC launch power is aggravated in presence of clock-gates.
Comparisons Across the Pattern Set

- LOC vs LOS power comparison done across the complete pattern set (first5 mid5, last5)
  - Clock gates present (No compression)
- LOS launch power significantly higher (~66% for the most power consuming pattern) than LOC launch power across the pattern set
## Root Cause Analysis

- Sequential power in LOS launch is around 100% more than LOC launch.

- Clock tree power for LOS launch is around 100% more than LOC launch.

- This indicates that nearly half the clocks are not active in LOC launch compared to LOS launch.

- LOC Launch: 38% flops get clocked

- LOS Launch: 100% flops get clocked

<table>
<thead>
<tr>
<th>Ckt1a</th>
<th>Clock Power (mW)</th>
<th>Comb. Power (mW)</th>
<th>Seq. Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOC launch</td>
<td>105</td>
<td>407</td>
<td>268</td>
</tr>
<tr>
<td>LOC capture</td>
<td>88.2</td>
<td>274</td>
<td>177</td>
</tr>
<tr>
<td>LOS launch</td>
<td>205</td>
<td>577</td>
<td>515</td>
</tr>
<tr>
<td>LOS capture</td>
<td>115</td>
<td>347</td>
<td>257</td>
</tr>
</tbody>
</table>
Clock Gate Hookup in Current Designs

LOC Launch: Clock to the FF through the functional path

FF may or may not get the launch clock depending on the functional enable (EN) of the clock gates.

LOS Launch: Clock to the FF through the Test path

FF will definitely get the launch clock. Only capture clock will depend on the functional enable (EN) of the clock gates.
Reduction Techniques

- Can be classified into two broad categories
  - ATPG techniques
    - Fill options
    - Low effort ATPG.
  - Design techniques
    - Clock gates TE control
    - Clock gates FE control
    - Low compression
1. Reduction Techniques : Fill

- **Ckt1a : Netlist without compression**
  - LOS launch power ~44% greater than LOC launch power for Adjacent fill and 0 fill techniques

![Effect of fill techniques on LOS launch for non-compression inserted netlist](image-url)
1. Reduction Techniques : Fill

- Ckt1b : Netlist with compression
  - LOS launch power for the most power consuming pattern ~90% higher than LOC launch

![Graph showing the effect of fill techniques on LOS launch for compression inserted netlist.](image-url)
2. Reduction Techniques: Modified LOS

- 100% flops get clocked during LOS launch
- 38% flops get clocked during LOC launch
- Changing the LOS clocking for Launch (make it similar to LOC clocking)

**Waveform for LOS**

- Pulsed based on EN value after last shift
- Pulsed based on EN value after n+1 shift

CLK
SE
EN
TEN_CG

DON'T CARE
Reduction Techniques: TE control of clock gates and adjacent fill

- **Ckt1a**: Netlist without compression
  - For the most power consuming pattern LOS launch is ~18% higher than LOC launch

![Graph showing power consumption for LOS and LOC launches with 18% difference](image-url)
Reduction Techniques: TE control of clock gates and adjacent fill

- Ckt1b: Netlist with compression
  - For the most power consuming pattern, LOS launch is ~30% higher than LOC launch
3. Reduction Techniques : FE control of clock gates

- ICG cell modified to include extra gate and input TE_new
- FE control of clock gates controlled during at-speed cycles
- If TE_new = ‘1’ only then functional value propagates
- This enables user to activate only certain groups of functional enables to allow propagation of clocks
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3. Reduction Techniques : FE control of clock gates and adjacent fill (contd..)

<table>
<thead>
<tr>
<th>Activation</th>
<th>Pattern Count</th>
<th>Peak switching activity</th>
</tr>
</thead>
<tbody>
<tr>
<td>All four groups allowed to toggle</td>
<td>4400</td>
<td>6700</td>
</tr>
<tr>
<td>One group at a time followed by all four</td>
<td>5483</td>
<td>6364</td>
</tr>
<tr>
<td>Two groups at a time followed by all four</td>
<td>7608</td>
<td>6072</td>
</tr>
<tr>
<td>One group at a time followed by two followed by four</td>
<td>8590</td>
<td>5905</td>
</tr>
<tr>
<td>Two groups at a time followed by three followed by four</td>
<td>7890</td>
<td>5363</td>
</tr>
</tbody>
</table>

Progressive Group Activation

Suitable for regenerating high switching patterns, after the other low power DFT/ATPG techniques have been applied.
4. Low compression and low effort ATPG

- Generate patterns with TE control and adjacent fill
- Examine the power profile of patterns
- Identify the high power consuming patterns
- Retarget the faults covered by those patterns with two low power alternatives
  - low compression
  - low effort ATPG
Pattern Generation for compression netlist with TE control and adjacent fill

First 1000 patterns
Max switching activity ~ 5700
Retarget with Low compression and low effort ATPG
Consolidated Flow

Input Design

- Insert dual compression codec
- Provide TE and FE controls to clock gates

Design Preparation

- Run ATPG (High Compression, Adj Fill, TE Control Enabled)
- Power Estimation (Toggle Count)
- Prune high switching patterns

Pattern regeneration:
- Low compression and low ATPG effort

Power Estimation (Toggle Count)

- Prune high switching patterns
- Updated Fault DB

Pattern regeneration:
- Progressive enabling of clock gate FEs

Gate Level Power Estimation

- Final Power Profile
- Updated Fault DB
- Threshold
- Threshold
Conclusions

- LOS launch power ~95% (for the most power consuming pattern) higher than LOC launch power.
- Several techniques proposed for TFT power reduction
- Adjacent Fill + TE Controls
  - LOS launch power ~18% higher than LOC launch
  - Pattern volume inflation for Ckt1a and Ckt1b was 21.8% and 52.8%, respectively.
- FE controls
  - LOS launch power comparable to LOC launch power.
  - The final pattern volume inflation after applying this technique on the reduced fault set (for the high switching patterns) for Ckt1b was ~59%.