DC Transfer Curve

And its applications
Basic Transistor Equations

\[ \beta = \mu C_{ox} \frac{W}{L} \]

\[ V_{GT} = V_{gs} - V_t \]

\[ I_{ds} = \begin{cases} 
0 & V_{gs} < V_t \quad \text{Cutoff} \\
\beta (V_{GT} - V_{ds}/2) V_{ds} & V_{ds} < V_{dsat} \quad \text{Linear} \\
\frac{\beta}{2} V_{GT}^2 & V_{ds} > V_{dsat} \quad \text{Saturation}
\end{cases} \]
DC Transfer curve

Relation between $V_{out}$ and $V_{in}$ under DC conditions
Graphical Approach

(b) $I_{dsn}$, $|I_{dsp}|$

$V_{in0}$, $V_{in1}$, $V_{in2}$, $V_{in3}$, $V_{in4}$, $V_{in5}$

$V_{out}$, $V_{DD}$
The transfer curve

Transistor’s regimes of operation
Current drawn from supply

\[ I_{DD} \]

\[ V_{in} \quad V_{DD} \]
Beta ratio effects

\[ \frac{\beta_p}{\beta_n} = 0.1 \]

\[ \frac{\beta_p}{\beta_n} = 10 \]

\[ \frac{\beta_p}{\beta_n} = 2 \]

\[ \frac{\beta_p}{\beta_n} = 1 \]

\[ \frac{\beta_p}{\beta_n} = 0.5 \]
Vinv: Inverter Trip Point

\[ \frac{\beta_p}{\beta_n} = 0.1 \]

\[ \frac{\beta_p}{\beta_n} = 10 \]

\[ \beta_p \]

\[ \beta_n \]

\[ V_{in} \]

\[ V_{out} \]

\[ V_{DD} \]

\[ Vinv \]

\[ V_{DD} \]

\[ 0 \]

\[ 0.5 \]

\[ 1 \]

\[ 2 \]
Vinv calculation

\[ I_{dn} = \frac{\beta_n}{2} \left( V_{inv} - V_{tn} \right)^2 \]

\[ I_{d\phi} = \frac{\beta_{\phi}}{2} \left( V_{inv} - V_{DD} - V_{t\phi} \right)^2 \]

\[ r = \frac{\beta_{\phi}}{\beta_n} \]
$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn} \sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}}$
Skewed Inverters

\[ \frac{\beta_p}{\beta_n} = 0.1 \]

\[ \beta_p = 10 \]

Lo-Skew

Hi-Skew

\[ V_{DD} \]

\[ V_{out} \]

\[ V_{in} \]

\[ V_{inv} \]
Process Variations

• Threshold voltages are random variables
  – Gaussian pdf is a good approximation

• Consequentially, inverter trip point (V_{inv})
  – Is also a random variable
  – As are other characteristics which depend on threshold
Voltage to logic levels

![Graph showing voltage to logic levels with labels V_{out}, V_{DD}, V_{OH}, V_{OL}, V_{tn}, V_{IL}, V_{IH}, V_{DD} - V_{DD}, and V_{in}. Unity Gain Points with slope = -1. Circuit diagram with symbols for V_{in} and V_{out}.]
Noise Margin Definitions

**Output Characteristics**
- Logical High Output Range
  - $V_{OH}$
  - $NM_H = V_{OH} - V_{IH}$
- Logical Low Output Range
  - $V_{OL}$
  - $NM_L = V_{IL} - V_{OL}$

**Input Characteristics**
- Logical High Input Range
  - $V_{DD}$
- Logical Low Input Range
  - $GND$

Indicates tolerance to noise
Why is there noise?

• DC Noise due to static voltage drops in the power grid

• AC noise:
  – due to coupling of switching signals
  – Transients in power grid
Importance of gain

• Larger gain better noise margin
• Restoring effect of logic levels in a long chain
• Large $V_t$ – better gain
Static Noise Margin for Memory Cell

Butterfly Diagram

SNM = 0.32 V