Design of Synchronous Buck Converter Employing an Adaptive Zero Voltage Switching for Ultra Low Power Systems

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Abstract

We investigate the design of a DC-DC buck converter for ultra low power applications like the sensors nodes of a Wireless Sensor Network. A Pulse Frequency Modulated (PFM) controller with Zero Voltage Switching (ZVS) is typically employed for very low load currents of less than 50mA. We propose an adaptive technique to implement Zero Voltage Switching (ZVS) and Inductor current sensing under dynamic load conditions, using clocked comparators. The low power comparators along with adaptive timing control minimize losses to improve the efficiency of the converter to 74% which is 10% higher than the previously reported discontinuous mode buck converters, Stratakos (1997), Zhou and Rincón-Mora (2006), Musunuri, et. al (2005), of less than 1mW range.

Keywords: DC-DC Converter, Low Power

1. Introduction

Recently, new ultra low power applications like wireless sensor networks have emerged, which consume very low currents of less than *20mA*, yet need a regulated efficient supply. Design of efficient DC-DC switching converters for such low currents will be challenge as the previously neglected loss mechanisms in controllers like the comparators and the mis-timing of the switching waveforms become very important. The basic approach followed in most of previous techniques (*Zhou and Rincón-Mora (2006), Long (2006), Dancy et. al (2000))* is to employ large Filter Inductor(L_f) to ensure continuous mode operation. The drawback of this technique is that it is designed to obtain good efficiency for a particular load range and if the load decreases below this range, the converter moves into a discontinuous mode thereby introducing losses.

Stratakos(1997) employs PFM (pulse frequency modulation) technique for low load currents. But this technique suffers from low efficiency due to static currents in the comparators as well their sluggish response.

The authors in *Long et. al (2006)* employ clocked comparators, but the sampling clock operates at frequencies in GHz range. The overhead of using fixed high frequency clocks is not significant in large load conditions, but for low load

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operations we are interested in, the clocks to the comparators can lead to substantial reduction of efficiency.

We will next cover some basic concepts for DC-DC Buck converters and highlight the loss mechanisms not addressed in prior work, which are of relevance at ultra low currents in Section 2. In Section 3 we describe a technique to implement ZVS via voltage and inductor current sensing using clocked comparators and show how one can use low frequency sampling clocks with adaptive timing adjustment to obtain good efficiencies. We discuss our simulation results in Section 4 followed by our conclusions in Section 5.

2. Design considerations of DC-DC Buck Converters for low load currents

The basic concepts and working of DC-DC Buck Converters are well documented in *Stratakos (1997)*, *Kursun et. al. (2003)*. It essentially consists of an inverter M_p, M_n, which connects its output node, V_x, to either the positive supply or ground (Fig. 1). The switching waveform at V_x is filtered by a low pass filter made up of the inductor L_f and capacitor C_f. The gate inputs to the NMOS and PMOS have to be precisely controlled in order to obtain the desired output voltage under varying load and input supply conditions. The major losses in such a converter are due to the conduction losses in the transistors and filter elements, through current losses when both transistors are simultaneously On, switching losses to drive the gates of the transistors and losses in the controller which generates the timing waveforms for the transistors.

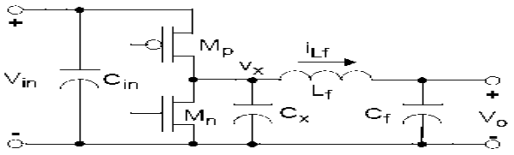


Fig. 1: A DC-DC buck converter

We will next discuss some of the design considerations and loss mechanisms in greater detail.

2.1 Conduction Mode

The mode of operation (continuous or discontinuous) of converter for entire load range is an important design issue which determines the selection of switching frequency of operation, filter inductor and design of controller circuit. The converter where the inductor current remains above zero for the entire cycle is called continuous conduction converter. To ensure continuous conduction mode the value of L_f and f_s (switching frequency) should be appropriately chosen. Typically for *1 MHz, 1mA* converter the filter inductor works out to be around $350\mu H$. This large value prohibits use of integrated On-chip inductors which are available only in the nano-henry range. In ultra low power applications, the load currents can vary dramatically between active and stand by modes of operation of the device. Hence, the converter will very likely slip into a discontinuous

mode of operation resulting in drastic decrease in efficiency (*Zhou and Rincón-Mora (2006)*, for such applications, converters are designed to work in discontinuous mode. But in this mode it is important to control the timing of the signals to the switching transistors. This usually requires circuits to sense the inductor current, so that the NMOS can be shut down upon the reversal of the inductor current to prevent losses. Various current sensing circuits have been proposed in *(Leung et. al. (2005), Forghani-zadeh and Rincón-Mora (2002))*. In *Leung et. al. (2005)*, the authors tap a small fraction of the current from the V_x node and use a current sense amplifier to measure the current. These amplifiers are analog amplifiers and need biasing currents for operation and hence contribute to loss of efficiency. In *Forghani-zadeh and Rincón-Mora (2002)*, the authors propose a *gm-C* cell based current sensor, which also suffers from a similar problem. We discuss an alternative current sensing scheme which uses a clocked comparator in Section 3.

2.2 Zero-Voltage Switching

Switching of the output node V_x of the buck converter can potentially lead to power loss proportional to $C_x \times V_i^2 \times f_s$, if attention is not paid to when the transistors are switched, which is what happens in a hard switched converter. In contrast, in a soft-switched converter, this internal node is switched in a relatively low loss fashion using the current flowing in the inductor itself. Here the MOS transistors are turned On only when their drain-source voltage is close to *0* and hence this technique is also called Zero Voltage Switching (*Stratakos (1997))*.

To achieve full benefit of ZVS, precise timing control for turning On of the NMOS and PMOS transistors is required and an appropriate dead time has to be provided between the two signals. When there is no dead time, short circuit current flows through the two transistors between external power and ground leading to power loss. If the dead time is too long, the body diode of the NMOS transistor supports the current conduction, again leading to a large loss as the diode turn on voltage is rather large. If the dead time is too short, then there will be capacitive switching losses.

The solution to this problem is to sense the voltage at the node V_x and turn On the switching transistors only when the concerned V_{ds} is '*0' (Stratakos (1997)*). This requires a voltage comparator which will sense the voltage at that node. As discussed in the previous section, analog comparators suffer from static current losses as well as slow operation. *Long et. al. (2006)* instead uses clocked comparators with high speed sampling clocks. For this approach to work well, sampling clock frequency has to be very high as otherwise, uncertainty of even one clock cycle leads to large losses due to conduction via the body diode. But high frequency sampling clock leads to unacceptably large power overheads for ultra low power operations. In the next section we will show how a low frequency sampling clock for the clocked comparator can be adaptively generated.

2.3 Output Filter Design

For the discontinuous mode of operation, the minimum value of inductor is determined by condition that the inductor current should not decay to negative value before node voltage V_x reaches zero. This is illustrated in Fig. 2 where the inductor current flows (positive direction) for duration(A-B) after V_x node voltage has crossed zero. If the inductor value chosen is less than minimum required, the inductor current will decrease to less than zero before V_x node voltage has crosses zero and ZVS cannot be achieved. In general, the inductor values obtained for discontinuous mode are lower than that for the continuous mode, thus allowing the possibility for future designs to implement completely monolithic converters with on-chip inductors for ultra-low power applications.

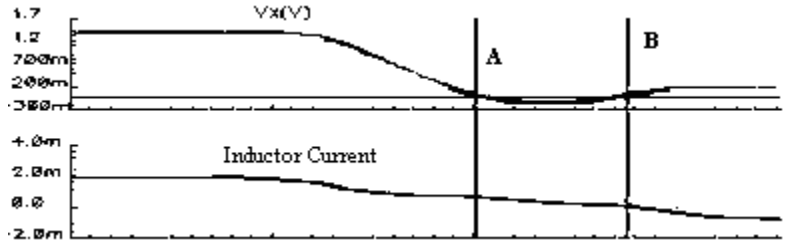


Fig. 2: Minimum duration for Inductor current reversal

The output filter capacitor is selected to ensure that its impedance at the switching frequency, including its equivalent series resistance , is small relative to the load impedance and capacitor's value should be large enough to source load current when both the Power FETs are Off .

2.4 Pulse frequency Modulation(PFM)

In ultra low power operation, the frequency related losses in the controller dominates the total losses, hence decreasing frequency of switching is a viable method to reduce losses. One control scheme which achieves high efficiency over a wide load range is pulse-frequency modulation (PFM) *(Stratakos (1997))*. In this scheme the converter is operated only in short bursts at light load. Between bursts, both power FETs are turned off, and the circuit idles with zero inductor current. During this period, the output filter capacitor (C_f) sources the load current. When the output is discharged to a certain threshold below V_{REF}, the converter is activated for another burst, returning charge to C_f. Thus the load-independent losses in the circuit are reduced.

3. Proposed Design of Buck Converter for ultra low power Motes

Our design is a combination of PFM and ZVS techniques. Fig. 3 shows the block diagram of our converter.

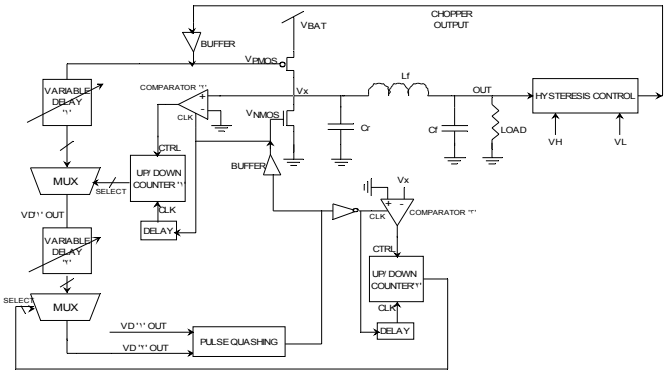


Fig. 3: Proposed Buck Converter with PFM control and adaptive ZVS scheme

It essentially consists of the standard buck converter elements like the switching PMOS and NMOS transistors and the LC filter of Fig. 1 and also includes three control loops. The loop with Comparator '1', is the basic PFM control loop (*Stratakos (1997)*). The PFM comparator '1' has two levels of comparison V_H and V_L, selection of which decides the ripple in the output voltage. The PMOS is turned On when the load voltage falls below V_L and is turned Off when it rises above V_H, thus regulating the load voltage.

The control loop with comparator '2' controls the when the NMOS is turned On and implements the adaptive dead time control to enable efficient ZVS switching of the NMOS.

The control loop with comparator '3' effectively implements inductor current sensing and determines when the NMOS is turned Off and enables implementation of efficient discontinuous mode operation.

The comparators used are clocked comparators as shown in Fig. 4 as it has a low clock to output delay *(Vijay and Amrutur (2007))*. It uses a single clock to trigger the comparison followed by a RS latch. The power consumed and the delay in this comparator is much less than a static analog comparator. We will next discuss how the sampling edge for the comparators '2' and '3' are generated adaptively.

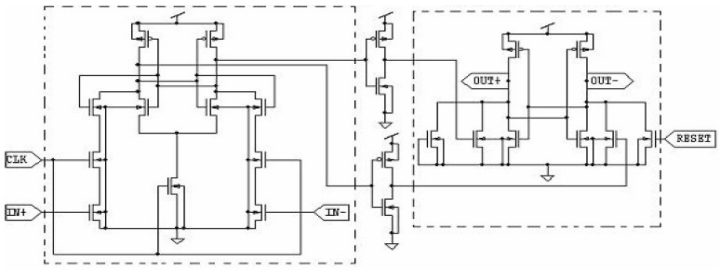
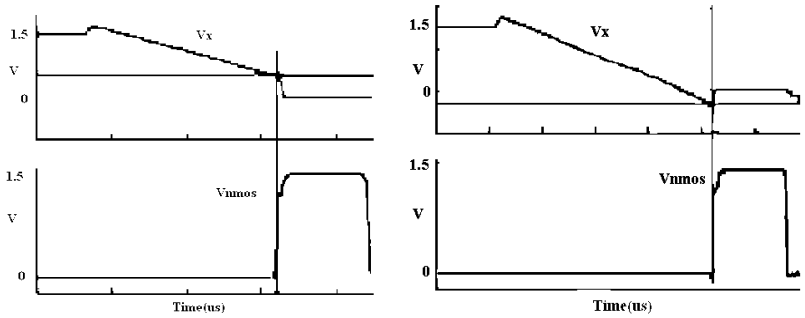


Fig 4: Clocked comparator *(Vijay and Amrutur (2007))*.

3.1 NMOS Switch ON control

The timing of NMOS turn On is critical in achieving high efficiency. Fig 5 (a) and (b) depicts losses due to timing errors.



(a) (b)

Fig 5: a) Dead time too short: Capacitive Switching loss, b) Dead time too long, body diode losses.

The control loop in Fig 3 implements an adaptive self learning technique which adjusts the timing of sampling clock to comparator '2' such that at the turn On of the NMOS, the V_x node is close to ground thereby reducing the switching and body diode losses. The output of comparator '1' is buffered and given to the gate of the PMOS switch. The NMOS switch needs to be turned On after a small delay after the PMOS switch is turned Off. This can be done by feeding the output of comparator '1' is to variable delay line, whose delay is adjusted by the feedback loop based on the values seen by comparator '2'. This delayed output is given simultaneously to NMOS switch as well as the clock input to Comparator '2'. Thus the comparator makes a comparison between V_x and a ref voltage V_{rx} (*0v* in this case) and outputs a digital value which is fed to an Up/Down counter which controls the variable delay line. When V_x voltage is above V_{rx}, the comparator causes the counter to increment by one which results in a slight increase in the dead time. When V_x is less than V_{rx}, the dead time is reduced. The timing of switching On the NMOS settles to a value which corresponds to V_x value being close to $\pm V_{rx}$, thereby minimizing switching and diode losses. Since this scheme derives the sampling clock from the PFM loop itself, its frequency is in the 1Mhz range and is much reduced compared to the 1.6 GHz clock used in *Long (2006)*. The voltage at node V_x when the loop stabilizes is shown in Fig 6, showing that V_x is close to *0* achieving ZVS.

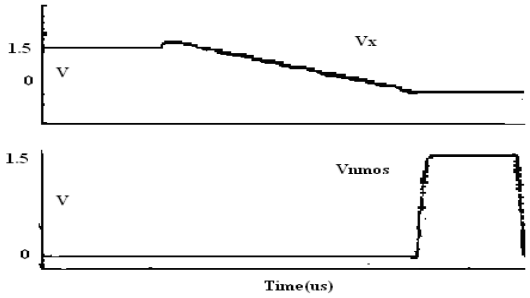


Fig 6: Adaptive dead time control to implement ZVS for NMOS turn ON.

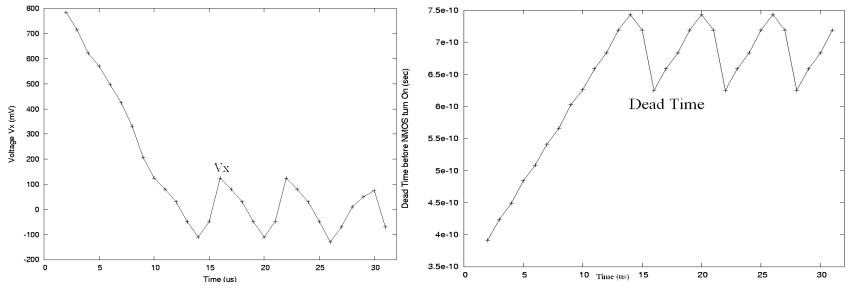
3.2 NMOS Switch OFF control

Unlike PWM continuous mode converters where NMOS turn Off is controlled by the next pulse to PMOS (with some delay), in discontinuous mode converters

the NMOS has to be turned Off on reversal of inductor current . As discussed earlier, prior work in inductor current sensing uses analog comparators *(Leung et. al. (2005), Forghani-zadeh and Rincón-Mora (2002))* which have static bias currents. Here we use a similar concept as above using clocked comparators to achieve NMOS turn Off. It takes advantage of the fact the V_x voltage changes to positive from negative when the inductor current reverses. In this circuit, the delayed output which is fed as comparator'2' clock is also fed to variable delay '2' and then to a chopper circuit , the role of this variable delay is to determine the period for which NMOS will be turned On. This is decided by feeding the output of the variable delay '2' as clock to comparator '3' and making the comparison of V_x to *Gnd*. The output of comparator is given to Up/Down counter to increase or decrease the NMOS pulse as the case may be. The chopper circuit then switches the NMOS Off. The circuit then idles with zero inductor current. During this period, the output filter capacitor sources the load current.

4. Simulation Results

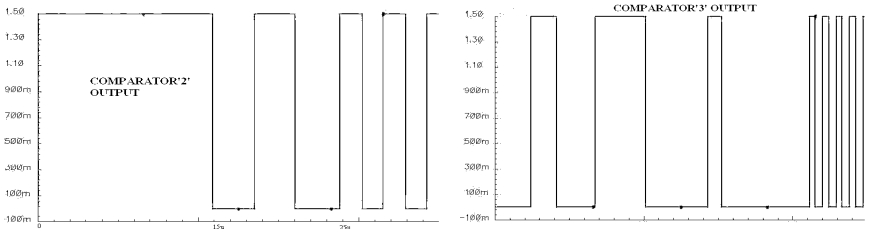
We have simulated the circuit of Fig 3 in *UMC 0.13-µm* RF CMOS technology using *Spectre RF*. Input voltage of *1.5V* was assumed considering the available Li Ion button cells .The voltage is down converted to voltage of *800mV*.



(a) **(b)**

Fig. 7: a) Value of V_x when NMOS turns On for dynamic loads of *800* Ω and *400*Ω . **b)** Variation in dead time for NMOS turn On with time.

It can be observed from Fig 7(a) that V_x node voltage during NMOS turn On settles between -110mV to 125mV for *800Ω* and -70mV to 135mV for *400 Ω* load , which is substantially less than 785mV at the start of conversion, implying reduction in switching losses in the same proportion.
Similarly the NMOS is turned Off when inductor current is between *-350µA* to *426µA* .
Fig 8(a) and (b) shows the output of comparator '2' and '3' respectively , the toggling of the output indicates the loop has settled to value +/- of the Ref value. The change in frequency is indicative of change in load from *800Ω* to *400Ω* .
The efficiency of 74% was obtained using the above technique which is more than 10% higher in comparison to 56% in *(Stratakos (1997))* , 53% in *Musunuri, et. al (2005)* and 64% in *Zhou and Rincón-Mora (2006)*.



(a) (b)

Fig 8 (a) Comparator '2' output (b) Comparator '3' output

5. Conclusion

This paper presents a design of a ultra low power synchronous PFM buck converter employing an adaptive self learning technique to implement Zero Voltage Switching(ZVS) and Inductor current sensing. This scheme uses clocked comparators and derives the sampling clocks from the PFM control loop signal via adjustable delay lines. The control loops adjust the timing of the sampling clocks to the comparators so that the dead time as well as NMOS turn Off for discontinuous mode are controlled and ZVS can be implemented achieving 74% efficiency for sub 1mW range Buck Converter .

6. Acknowledgements

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7. References

[1] A J Stratakos (1997), High-Efficiency Low-Voltage DC-DC Conversion for Portable Applications, Ph D Thesis, University of California, Berkeley, 1997.

[2] S Zhou and G A. Rincón-Mora (2006), A High Efficiency, Soft Switching DC-DC Converter with Adaptive Current Ripple Control for Mobile, Circuits and Systems II, IEEE Transactions on, Vol. 53, Apr. 2006, 319-323.

[3] C Long, S Reddy, S Pamarti, L He and T Karnik (2006), Power-Efficient Pulse Width Modulation DC/DC Converters with Zero Voltage Switching Control, ISLPED, Oct. 2006, Tegernsee, Germany, 326-329.

[4] V Kursun, S G. Narendra , V K. De and E G. Friedman (2003), Analysis of Buck converters for On-chip Integration with a dual supply voltage µprocessor, IEEE Transactions on VLSI Systems, Vol. 11, June 2003, 514-522.

[5] A P. Dancy, R Amirtharajah and A P. Chandrakasan (2000), High-Efficiency Multiple-O/p DC–DCConversion for Low-Voltage Systems", IEEE Transactions on VLSI Systems, Vol. 8, No. 3, June 2000, 252-263.

[6] C Y Leung, P K. T. Mok, K N Leung, and M Chan (2005), An Integrated CMOS Current-Sensing Circuit for Low-Voltage Current-Mode Buck Regulator, IEEE Transactions on Circuits and Systems II, Vol. 52, No. 7, Jul. 2005, 394-397.

[7] H P Forghani-zadeh and G A. Rincón-Mora (2002), Current Sensing Technique for DC-DC converters, Circuits and Systems, MWSCAS-2002, Aug. 2002, II-577-580.

[8] S Musunuri, P L. Chapman, J Zou, and C Liu (2005), Design of low power Monolithic DC–DC Buck Converter with integrated inductor, Power Electronics Specialists Conference, PESC' 05, IEEE 36th, 2005.

[9] U.K Vijay and B. Amrutur (2007), Continuous Time Sigma Delta Modulator Employing a Novel Comparator Architecture, VLSI Design 2007, 20th International Conference on, Jan. 2007, 919 – 924.