Stable SRAM Cell Design for the 32 nm Node and Beyond

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Abstract

SRAM cell stability will be a primary concern for future technologies due to variability and decreasing power supply voltages. 6T-SRAM can be optimized for stability by choosing the cell layout, device threshold voltages, and the ß ratio. 8T-SRAM, however, provides a much greater enhancement in stability by eliminating cell disturbs during a read access, thus facilitating continued technology scaling. We demonstrate the smallest 6T ($0.124\mu m^2$ half-cell) and full 8T ($0.1998\mu m^2$) cells to date.

Introduction

As memory begins to dominate chip area in high performance applications, SRAM has become the focus of technology scaling [1,2]. Traditionally, SRAM cell size has scaled in accordance with technology ground rules; however, with the growing importance of variability, it is feared that this may no longer be possible. Because minimum gate length and width devices are used to minimize cell area, SRAM is most susceptible to both process-induced variations in device geometry as well as threshold voltage variability due to dopant fluctuations [3]. In addition, the impact of variability is most pronounced in SRAM because cell operation, which depends upon well-matched FETs, must be satisfactory for each individual cell (no averaging across multiple stages as in logic). The fundamental concern of cell stability [4], which determines minimum array operating voltage and yield, has thus become increasingly difficult to address.

In this work, SRAM (half) cells with areas down to $0.124\mu m^2$ [1] provide the unique opportunity to study device set points to maximize cell stability. The device structure (25nm SOI, 15nm spacer, single-implant S/D, 12nm $CoSi_2$) is chosen to accommodate aggressively scaled SRAM. Ground rules are scaled in accordance with process capabilities to achieve different cell areas.

As SRAM is scaled, sufficient static noise margin (SNM) becomes difficult to maintain (Fig. 1) due both to increased variation and shifting of device characteristics from design targets (conceptually, these are equivalent to noise). In particular, mismatch between the reflected SNMs of the two halves of a cell is enhanced (Fig. 2) due to aggressive ground rules and dopant fluctuations. In addition, narrow-width or short-channel effects degrade SNM by distorting inverter transfer characteristics.

6T-SRAM Cell Optimization

SRAM cell layout can be optimized to minimize variability by converting the "Thincell" [5] active pattern to a straight line layout (eliminating jogs and corners, thereby increasing reliance on metal interconnect). This facilitates lithography and reduces sensitivity to overlay errors, which improves mismatch and critical dimension control, thus increasing SNM (Fig. 3).

The cell ß ratio (Fig. 4) balances performance, stability, and area. For stability, increasing ß (thus growing the cell size) reduces the disturb voltage on the "0" node of the cell and lowers the switch point of the cross-coupled inverters (Fig. 5). The two mechanisms have opposing effects on SNM and result in an optimum stability for ß~2-3 (Fig. 6). Since ß has very little impact on SNM in this range, ß~2 may be desired to minimize cell area.

A low pFET V_T for the pull-up device and high nFET V_T for the pass-gate device are desirable to maximize SNM (Fig. 7), though both result in degraded performance. By setting ß=2, further adjustment of the nFET pull-down V_T has little impact on SNM (Fig. 8). Thus, it is practical to set it to be the same as the nFET pass-gate V_T (i.e. to minimize nFET narrow-width effect).

Functional SRAM cells down to $0.143\mu m^2$ [1] and half-cells down to $0.124\mu m^2$ (Fig. 9) in cell area were fabricated. Ground rules for $0.124\mu m^2$ cells are similar to [1], except for shorter gate lengths (35nm) and tighter overlay margins. ß=1 minimizes cell size, but degrades SNM by increasing the read disturb voltage.

An 8T-SRAM Cell with Improved Stability

The fundamental stability problem in 6T cells is that in the read condition, a pass-gate pulls the "0" storage node up to a non-zero value (circled in Fig. 10a). Adding two FETs to a 6T cell provides a read mechanism that does not disturb the internal nodes of the cell (Fig. 10b), thereby eliminating the worst-case stability condition. This requires separate read and write word lines and can accommodate dual-port operation with separate read and write bit lines. Without read disturbs, the worst-case stability condition for an 8T cell is that for two cross-coupled inverters, which provides a significantly larger SNM (Fig. 11). A dramatic stability improvement can thus be achieved without a tradeoff in performance since a read access is still performed by two stacked nFETs. An efficient layout for this cell is achieved by extending the gate shape for one inverter in a ß=1 6T cell (Fig. 12). This accommodates the additional FET stack at an area penalty of only ~30% as compared with a compact ß=2 6T cell. While other 8T configurations are possible, this cell is very layout efficient, provides the maximum SNM by decoupling cell nodes during read and write operations, and can even provide a performance advantage over 6T if the pass-gates and read stack are designed to be strong devices. 8T-SRAM cells have been fabricated down to $0.1998\mu m^2$ in area with improved SNM (Fig. 13). The 8T cell provides especially pronounced benefits at low V_{DD} (Fig. 14) even when 6T ground rules are relaxed.

Summary

SRAM cell design strategies have been discussed to maximize cell stability. While 6T-SRAM can be optimized for stability, much larger gains can be realized with 8T-SRAM cell. A ~30% area penalty is incurred with the addition of two extra FETs, but 8T-SRAM can allow for continued scaling beyond that which is possible with traditional 6T-SRAM.

Acknowledgements

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References

[1] D. M. Fried, et al., *IEDM*, 2004.
[2] F.-L. Yang, et al., *VLSI*, 2004.
[3] R. Keyes, *JSSC*, Aug. 1975, p. 245.
[4] E. Seevinck, et al., *JSSC*, Oct. 1987, p. 748.
[5] M. Khare, et al., *IEDM*, 2002.

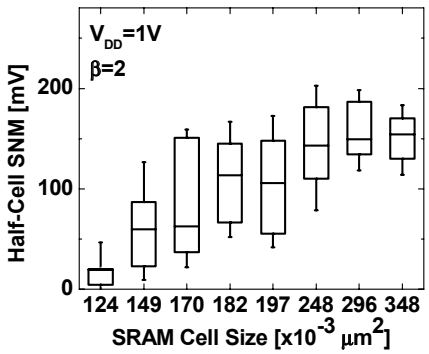


Figure 1: Cell stability decreases as SRAM cell size is scaled due both to variability and threshold voltage roll-off at small channel lengths and widths.

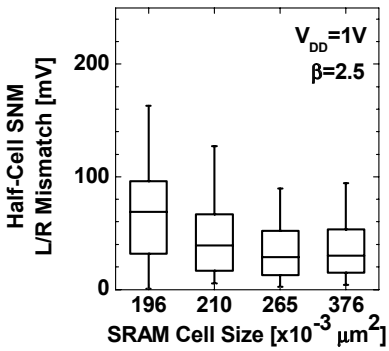


Figure 2: Mismatch between the two halves of an SRAM cell increases with scaling due to process variability and dopant fluctuations.

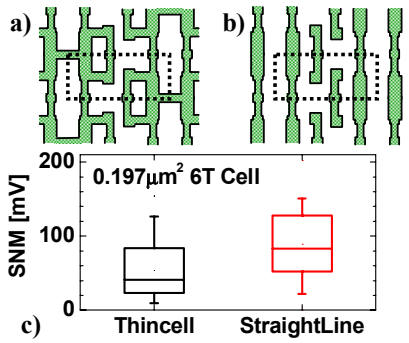


Figure 3: Active pattern for a) Thincell [5] and b) straight line layout. c) The straight line layout yields higher SNM.

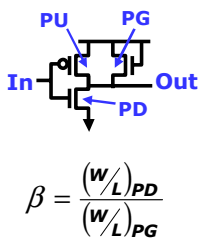


Figure 4: The β ratio measures the relative strengths of the pull-down and pass-gate nFETs.

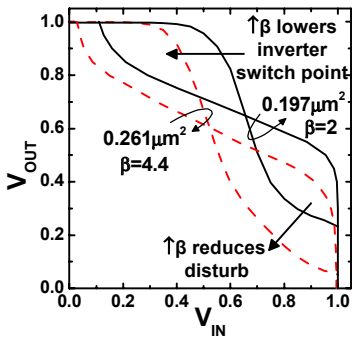


Figure 5: Increasing β simultaneously lowers the inverter switch point as well as the disturb voltage.

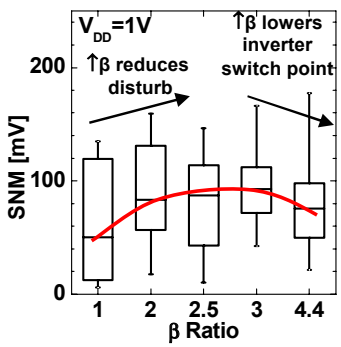


Figure 6: Optimal SNM lies at β ~ 2-3. Cell sizes range from 0.183μm^2 for β=1 to 0.261μm^2 for β=4.4.

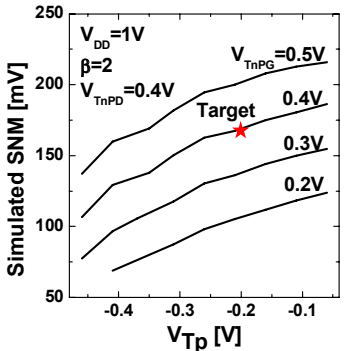


Figure 7: SNM is largest with a low (less negative) V_T pFET pull-up and a high V_T nFET pass-gate.

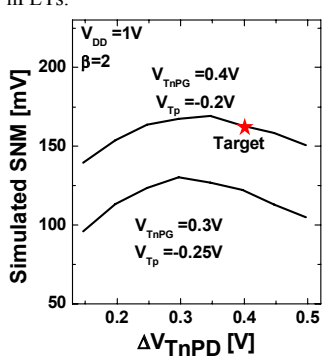


Figure 8: In the range of interest, V_T for the pull-down nFET does not significantly affect SNM.

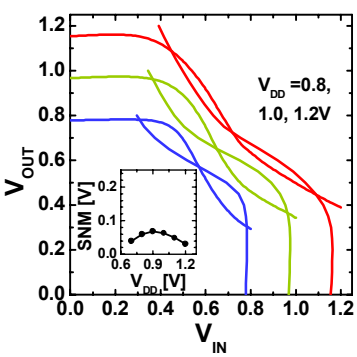


Figure 9: Half-cell butterfly curves at V_{DD} =0.8,1,1.2 V for a 0.124 μm^2, β=1 SRAM single cell test structure.

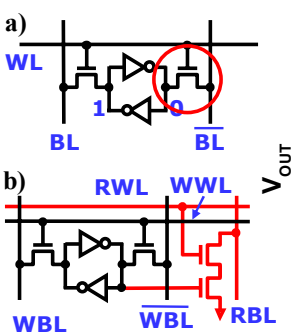


Figure 10: a) 6T and b) 8T-SRAM cell circuit diagrams.

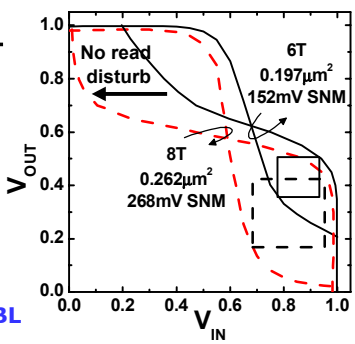
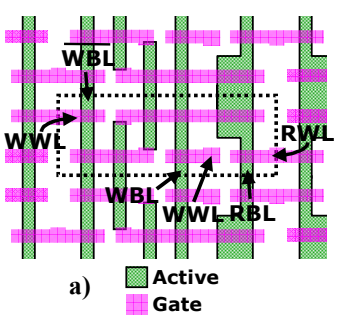


Figure 11: Butterfly curves show that SNM is enhanced for 8T cells due to elimination of read disturbs.



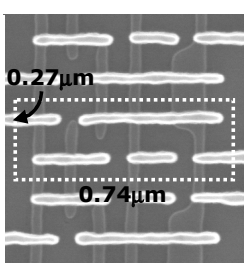


Figure 12: a) The layout of an 8T cell can follow the Thincell approach [5], thus resulting in a cell that is only ~30% larger than a β=2 6T cell. b) Top-down SEM of a 0.1998μm^2 8T-SRAM cell post-gate etch.

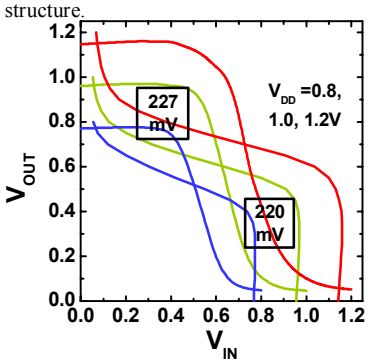


Figure 13: Butterfly curves at V_{DD}=0.8, 1.0, and 1.2 V for a 0.1998 μm^2 8T-SRAM single cell test structure. This is the smallest 8T cell ever reported.

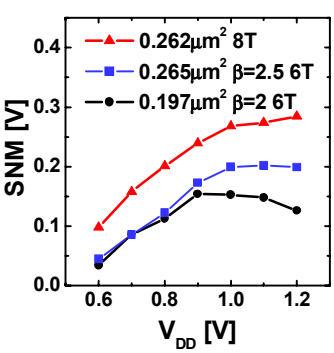


Figure 14: 8T shows enhanced SNM especially at low V_{DD} even when 6T ground rules are relaxed.