A 45nm SOI Embedded DRAM Macro for POWER7™
32MB On-Chip L3 Cache

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Outline

- Motivation
- Deep Trench Technology
- Macro Architecture
- 3T / 4T Micro Sense Evolution
- 6T Direct Sense and Extended Pre-Charge
  - 45% Power Reduction with only 1.7% Growth
- Hardware Results
- Summary
DRAM Motivation

- Density: ~3x Advantage over SRAM
- Power: 5x Lower Standby Compared to SRAM
- Soft Error Rate: 1000x lower than SRAM
- Performance: DRAM can have lower latency!

Requirements

- Integrated with Base Logic (without logic degradation)
  - Enables Library IP Reuse
- General Purpose Macro for Maximum DRAM IP Reuse
- Wide Operating Range for Voltage / Frequency Scaling
eDRAM Size/Latency Advantage

ISSCC’04 CPU

CPU with DRAM
(4x denser/2x slower)

Chip size
432mm² → 245mm²
(43% smaller)

* 39% decrease in wire delay to furthest L3-cache subarray

L3 Latency (normalized to 20 cycles)

<table>
<thead>
<tr>
<th></th>
<th>L3-Tag</th>
<th>L3-Cache</th>
<th>Wire Delay</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>5 cycles</td>
<td>5 cycles</td>
<td>10 cycles</td>
<td>20 cycles</td>
</tr>
<tr>
<td>eDRAM</td>
<td>5 cycles</td>
<td>10 cycles</td>
<td>6 cycles</td>
<td>21 cycles</td>
</tr>
</tbody>
</table>

Pilo

*23mm

*14mm

245mm²

23mm

14mm
eDRAM Size/Latency Advantage

45nm eDRAM vs. SRAM Latency

- eDRAM Total Latency
- SRAM Total Latency
- eDRAM Wire/Repeater Delay
- SRAM Wire/Repeater Delay

eDRAM Faster than SRAM

Memory Block Size Built With 1Mb Macros
Power7™ Processor

- 567mm²
- 32MByte on chip eDRAM
- 1.2B Transistors
  - Equivalent to 2.7B
  - eDRAM Efficiency
- Eight Processor Cores
- eDRAM ~11% Die Area
- Balanced Performance
  - Dual DDR3 Controllers
  - SMP Links
    - 20k Coherent Operations
  - 590 GB/s Total Bandwidth

Power7 Described in Sessions 5.4, 9.3 and 19.2 at ISSCC 2010
POWER7™ Chiplet

1Mbit DRAM Macro
- 32 Macro per Chiplet = 4MByte
- 8 Chiplet per Chip = 32MByte

Technology | 45nm PD SOI
---|---
Cell Size | 152nm x 221nm (0.0672µm²)
Macro Size | 377µm x 634µm (0.239mm²)
Organization | 1k row x 8 col x 146 (1Mbit)
Sub-Array | Hierarchical µSense
          | 264 word-line x 1200 bit-line
Macro Performance | 1.7ns/1.35ns (cycle/access)
          | @ 1.05V
SOI Deep Trench DRAM Cell

- WL
- BOX
- Deep Trench Cap
- BL
- Node
- Passing WL
- Strap
- Pass Device
- 18fF Storage Capacitor

4.0um
1Mbit Macro Architecture

- Word Lines (WL) Stitched with Metal 3 (M3)
- Master WL also Decode 1 of 8 Micro Arrays within Sub-Array
Memory Arrays are composed of Row and Columns

Most DRAMs use 1 Transistor as a switch and 1 Cap as a storage element (Dennard 1967)

Single Cell Accessed by Decoding One Row / One Column (Matrix)

Row (Word-Line) connects storage Caps to Columns (Bit-Line)

Storage Cap Transfers Charge to Bit-Line, Altering Bit-Line Voltage
DRAM 101: Cell Charge Transfer

\[ \Delta V = (V_{bl} - V_{cell}) \left[ \frac{C_{cell}}{C_{bl} + C_{cell}} \right] \]

Transfer ratio
DRAM Components of Cycle Time

DRAM is Destructive Read, Requires Write back (SRAM Does Not)
Short Bit-Line, High Transfer Ratio

TR = Transfer Ratio = \( \frac{C_{\text{cell}}}{C_{\text{cell}} + C_{\text{bl}}} \)

1. 2x Faster Charge Transfer (90%)
   
   \[ t = 2.3 R_{\text{dev}} \frac{(C_{\text{bl}} \cdot C_{\text{cell}})}{(C_{\text{bl}} + C_{\text{cell}})} \]

2. 2.3x More Signal

3. 10% More Write Back

Barth ISSCC 2007
eDRAM Performance Trends

- Random Cycle
- Access Time

Logic-Based eDRAM Process

Direct Reference Cell Write (ISSCC’02 9.3)
Early Write (ISSCC’03 17.5)

Direct Write (ISSCC’04 11.3)
2.2nm Device (ISSCC’05 11.4)

μ-Sense-Amp (ISSCC’07 27.1)

Access/Random Cycle (ns)

- DRAM Based
- 180nm
- 130nm
- 90nm
- 65nm
- 65nm
- 45nm SOI

Technology Node
**Micro Sense Architecture**

1 of 8 Micro Arrays (µ-Array) per Sub-Array

- Hierarchical Direct Sense
- Short Local Bit-Line (LBL)
  - 32 + 1 Redundant Cells per LBL
- 8 Micro Sense Amps (µSA) per Global Sense Amp (GSA)
- Write Bit-Line (WBL)
  Uni-Directional Write ‘0’
- Read Bit-Line (RBL)
  Bi-Directional Read / Write ‘1’
Micro Sense Hierarchy with Column Interleave

Local Data (M2) -> Upper Data Sense Amp (DSA) -> Global Data (M4)

1 of 8 Micro Array

Lower Data Sense Amp (DSA)
3T μSA Read Operation (ISSCC’07)

Nominal Process, 1v, 85c

Volts

-0.2 0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8

Time(ns)

0.0 0.4 0.8 1.2 1.6 2.0 2.4 2.8 3.2 3.6 4.0

Read ‘1’

WL0

Read ‘0’

WL1

Restore

Strong ‘1’

Strong ‘0’

Weak ‘1’

Weak ‘0’

3T μSA

Barth, ISSCC’07

32 DRAM Cells

Setp fires, refreshing ‘0’
μSA Evolution

3T - μSA
1. Write Zero (W0)
2. Write One (W1)
3. Read Head (RH)

No μ-Array Decode

4T - μSA
4. PFET Header (PH)
   - LBL Power Gate
   - LBL Leakage
   - Decoded Master Word-Line (MWL)

Partial μ-Array Decode

6T - μSA (new)
5. Pre-Charge (PC)
   - WBL Power (Write ‘0’ Only)
6. NFET Footer (NF)
   - RBL Leakage
   - Decompose Pre-Charge and Read Enable (MWL_RE)

Full μ-Array Decode

Power Reduction w/ Decode Increased Transistor Count

Barth, ISSCC’07
Klim, VLSI’08

32 DRAM Cells
Power 54fC/Bit

32 DRAM Cells
Power 33fC/Bit

33 DRAM Cells
Power 18fC/Bit

Read Enable

This Work
### µSA Control

<table>
<thead>
<tr>
<th>Function</th>
<th>3T</th>
<th>4T</th>
<th>6T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Enable</td>
<td>None</td>
<td>MWL_EQ</td>
<td></td>
</tr>
<tr>
<td>Pre Charge</td>
<td>WBL</td>
<td>WBL</td>
<td>MWL_RE</td>
</tr>
<tr>
<td>Read Enable</td>
<td>WBL</td>
<td>WBL</td>
<td></td>
</tr>
<tr>
<td>Write ‘0’</td>
<td>RBL</td>
<td>RBL</td>
<td>RBL</td>
</tr>
<tr>
<td>Write ‘1’</td>
<td>RBL</td>
<td>RBL</td>
<td>RBL</td>
</tr>
</tbody>
</table>

**3T**
- 32 DRAM Cells
- Power: 54fC/Bit
- Barth, ISSCC’07

**4T**
- 32 DRAM Cells
- Power: 33fC/Bit
- Klim, VLSI’08

**6T**
- 33 DRAM Cells
- Power: 18fC/Bit
- This Work

**Power Reduction w/ Decode**
- Increased Transistor Count
3T/4T GSA (old design)

1. NAND on WBL required for
   - LBL Pre-Charge
   - Write and Write-Back ‘0’
   - WBL Swings Every Cycle
   - Sinks RBL Discharge Current

2. Large EQ Device required
   - Absorb WBL Coupling When PRE Falls
6T GSA (new design)

8x μSA per GSA
Decoded with Master Word-Lines (MWL)

Simplification
1. WBL Only for Write / Write-Back ‘0’
   WBL No Longer Sinks RBL Load
2. Smaller EQ Device (No WBL Coupling)
Write Disturb

1 of 8 Columns Written

- - - - Write Aggressor
------------------------ Refresh Victims

GSA Written

Global Bit-Lines RBL/WBL Pairs

Disturb

Refresh

Upper Data Sense Amp

Global Sense Amp

Global Sense Amp

Global Sense Amp

Global Sense Amp

Lower Data Sense Amp
Coupling Mechanisms – Cross Section View

1. Write ‘1’ Couples WBL below Ground Increasing RH leakage during Refresh ‘0’
2. Write ‘0’ Couples RBL above VDD Delaying Feedback during Refresh ‘1’
3. Read ‘1’ Couples Half-Selected LBL Below GND Increasing Array Device Sub-VT Leakage
Extended GSA Pre-Charge

Release Pre-Charge on Upper GSA’s to avoid Write power burn

GSA Written

1 of 8 Columns Written

----- Write Aggressor

.............. Refresh Victims

Global Bit-Lines RBL/WBL Pairs

Adjacent Bits are Shielded with Extended Pre-Charge
All Other Bits Shielded by Column Interleave

Extend Pre-Charge on Lower GSAs to absorb Write disturb

Absorb

Refresh
**Read ‘1’ Simulation – Worst Case Slow Devices**

- **Wordline**: Adjacent WBL Write ‘0’ Disturb Absorbed by Extended Pre-Charge (Coupling #2)
- **Node**: 6T RBL 10% Faster
- **LBL**: 4T Unselected LBL (Coupling #3)
- **4T RBL**: Write ‘0’ Disturb
- **6T RBL**: 6T LBL Clamped = Improved Retention

**Graph Details**
- **X-axis**: Time (ns)
- **Y-axis**: Volts

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*IBM*
Read ‘0’ Simulation – High Voltage, Leaky Devices

- Extended Pre-Charge and Unselected Read Head Footers = More Read ‘0’ Margin

- Write ‘1’ Disturb Couples WBL Low
- No Leakage Impact for 6T (Coupling #1)

Volts

Wordline

Write ‘1’ Disturb

Node

- 64% More 0’s Margin
# Array Height Summary

<table>
<thead>
<tr>
<th></th>
<th>µSA 4T ⇒ 6T</th>
<th>GSA Simplification</th>
<th>Distributed Row Redundancy</th>
<th>Net</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tracks</td>
<td>+28</td>
<td>-16</td>
<td>-4</td>
<td>+8 (+1.7%)</td>
</tr>
</tbody>
</table>

**Bar Chart**

- **Tracks**
  - 4T: 60% (22% Row Red, 38% µSA)
  - 6T: 59% (27% Row Red, 32% µSA)

- **Net Change**:+1.7%

The bar chart visually represents the changes in array height due to different simplification techniques and redundancy measures.
Refresh ‘1’ Active Power Savings

• 4T Cuts Half-Selected LBL Power
• 6T Cuts WBL Power
DRAM Random Cycle Data (BIST)

- Random Cycle (ns)
- Array Supply (Volts)

- Pass: 1.7ns @ 1.05V
- Fail: 1.7ns @ 1.05V
DRAM Latency Hardware Data (BIST)

Latency (ns)

Array Supply (Volts)

1.35ns @ 1.05V

Pass

Fail
**Embedded DRAM Node Advantage**

<table>
<thead>
<tr>
<th></th>
<th>Poulson</th>
<th>P7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cores</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>L3 Cache</td>
<td>32MB SRAM</td>
<td>32MB eDRAM</td>
</tr>
<tr>
<td>Area</td>
<td>544mm²</td>
<td>567mm²</td>
</tr>
<tr>
<td>Node</td>
<td>32nm</td>
<td>45nm</td>
</tr>
</tbody>
</table>

**IBM Power7™**

Poulson

ISSCC 2011 Paper 4.9

IBM Power7™

ISSCC 2010 Paper 5.4
Summary

1Mbit Macro for Power7 On-Chip 32MByte L3 Cache

- Reviewed 3T/4T Coupling Mechanisms
- Introduced 6T Micro Sense
  - Reduced Bit-Line Refresh Power by 45% (vs 4T)
  - Layout Area Penalty Reduced to only 1.7%
  - Extended Pre-Charge absorbs write disturbs
    Improving 1’s Latency by 10% and 0’s Timing Margin by 64%
  - 1.35ns Access / 1.7ns Random Cycle Demonstrated

- 32nm Products Recently Announced
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