E0-284: Project: tiny-FPGA Design

In this project, you will design a tiny-FPGA in groups of 2.

Reference:
FPGA Architectures: Survey and Challenges, Kuon, Tessier, Rose.
Verilog HDL: Samir Palnitkar

The tiny-FPGA will have 4 Logic Clusters (LC) and 4 Programmable Routing Switch (PRS) blocks (Fig 5.3 from above reference). Each LC will have two BLE (Basic Logic Element), each of which has a 4-input LUT and a flop. The routing channel will have 4 wire segments in horizontal and vertical directions (see Fig 5.3), with input and output connection blocks (ICB, OCB) having Fc,in=Fc,out=4/4. The switch block will have Fs=3. The total number of IOs for the tiny-FPGA will be 16 (four on each side).

1. Architecture of the tiny-FPGA: Due: October 23 2013

Work out the block diagram of the tiny-FPGA in terms of all the major blocks and their interconnections (including the IOs), the internal structure of the LC/BLE, the programmable routing switch (PRS) block and the input and output connections blocks (ICB, OCB) and the IO Connection Block (IOCB). The IO Connection block will have the 16 Bi Directional IOs (configurable as input or output) and connectivity to connect to the internal routing channels.

Submit a short report with the
a) Block level diagram of the tiny-FPGA identifying all the blocks and their interconnections.
b) HDL module header indicating the inputs and outputs of the tiny-FPGA
c) Block level diagram of the LC and BLE.
d) HDL module header indicating the inputs and outputs of the LC and BLE modules
e) Block level diagram of the PRS
f) HDL module header indicating the inputs and outputs of the PRS module
g) Block level diagram of the Input and Output connections blocks.
h) HDL module header indicating the inputs and outputs of the Input and Output connections blocks.
i) Block level diagram of the IOCB
j) HDL module header for the IOCB

Note: block level diagram is not transistor level diagrams – but includes simple functional blocks like muxes, flops, sram blocks etc. and their interconnections. Don’t forget to include the configuration SRAM blocks and their IOs, which are needed to program the each of the muxes switches in these blocks.

2. HDL implementation and verification of the LC module: Oct 30 2013

a) Verilog/VHDL code for the LC module
b) Identify the list of tests you would do to test the module (in one line text form). For e.g.
   a. Read and write of configuration memory within LC
   b. Read and write of LUT 1 in LC
   c. Read and write of LUT 2 in LC
   d. Configuring LUT1 to flop output in LC
   etc.

c) Verilog/VHDL Code for the test bench for the module
d) Test outputs indicating functionality testing (waveforms or text output).

3. HDL implementation and verification of the PRS, ICB, OCB and IOCB modules and the entire tiny-FPGA: Due November 18 2013.

a) Verilog/VHDL code for PRS, ICB OCB, IOCB and the tiny-FPGA module.
b) Configuration memory pattern to implement a 4-bit ripple carry adder, with two 4-bit inputs and a 4-bit output with a carry.
c) Test bench to test the tiny-FPGA module to load the configuration memory to configure the mini-FPGA as a 4-bit ripple carry adder.

d) Simulation results for adding 256 different number pairs with input and output values.

4. Schematic & Layout of the 4-input LUT module: December 4 2013
   a) Transistor Schematic of the LUT module
   b) Layout of the LUT module including LVS and DRC checks
   c) Circuit level simulation of LUT module. Simulate the following pattern:

   ```
   write address=0 data=1
   write address=15 data=0
   read address=0
   read address=15
   ```

   Show waveforms and indicate timing delay for 1.0V operation using the 16nm process model

   Show a screen shot of the layout of the module and indicate the x and y dimensions.