1. For the following Boolean formula:

\[ Y = (A + B) \cdot C + B \cdot D \]

a) (2) Sketch the transistor level implementation of the CMOS gate (single stage).

b) (2) Mark the sizes of the transistors such that the pullup and pull down stack have the same drive strength as that of a unit inverter. (Unit inverter’s PMOS width=2, NMOS width=1). Assume all channel lengths are minimum.

c) (2) Write the logical effort for each of the inputs is:

2. (2) Assuming a DIBL coefficient of 100mV/V, if the supply voltage is reduced by 600mV, determine by what factor the leakage current at room temperature will reduce.

3. (2) Assume mobility changes with temperature, T (in K) as:

\[ \mu(T) = \mu(300K) * (300K/T)^2 \]

The threshold voltage at 300K is 350mV with a reduction of 1mV/K. Assuming perfect velocity saturation, find the gate voltage at which the saturation currents at 300K and 400K are equal.

4. For the circuit shown below:

a) (4) Sketch the model of just the interconnect portion you would use for circuit simulation to obtain delays to A, X and B, with reasonable accuracies for the slew rate and the 50-50% delay. Indicate the values of all the components on the sketch itself.

b) (2) Estimate the delay from S to A and B.

c) (8) Find the size of the repeater and the number of repeaters for each wire segment, to minimize the overall delay from S to A and B. Assume all transistors are minimum channel length of L=21nm and PMOS is \( \frac{1}{2} \) as strong as NMOS of same width.

d) (4) Design the buffering inside the box labeled with ?, to minimize the overall delay and report the number of stages and sizes for each stage.

5. (6) Consider the circuit below where the aggressor inverter is sized to have NMOS W/L=1um/21nm and PMOS W/L=2um/21nm.
Find the minimum size of the victim inverter such that the coupling voltage at node B is less than 20% of the supply voltage (VDD=1V). You may neglect the loading effects of the load inverters at A and B.

6. (2) For the waveform shown below, find the activity factor:

7. (6) Let PA=PB=PC=PD=0.5 be the probability that nodes A, B, C, D are 1. Assume that the probabilities are uncorrelated cycle to cycle. Find the activity factors for all the intermediate nodes in the figure below.

8. Assume that a logic block has 32K gates (including 500 flops at input of the block and 500 at the output). Let the capacitance per gate (for both a logic gate and a flop) be 1ff. Let the delay per gate at 1V be 20pS and this is also the delay for flop setup time and the clock to Q delay of the flop. Let the critical path length be 50gates (including flop setup and flop clock to Q).
   a) (2) Find the dynamic, leakage and total power of the circuit at the max operating speed. Assume leakage power is 1/3rd the dynamic power at this voltage and speed.
   b) (8) Assume threshold voltage is 0.25V and delay scales as k VDD/(VDD-VTH). The DIBL coefficient is 0.1 and body effect factor n=1.5 and thermal voltage is 25mV. Find the total power dissipation at the same operating frequency when an additional pipe stage is introduced (with an extra 500 flops), and supply voltage is reduced to be as small as possible to accommodate the speed.