Dynamic Voltage Scaling

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Max-Delay: Flip-Flops

Combinational Logic

\[ t_{pcq} < t_{pd} < t_{setup} < t_{skew} \leq T_c \]
Voltage – frequency space

Frequency

Voltage

500x
PVT Spreads

Frequency

Voltage

PVT Spread
# Variations

## Classification of Variations

<table>
<thead>
<tr>
<th>Spatial Reach</th>
<th>Temporal Rate of Change</th>
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<tr>
<td>Local</td>
<td>Extremely Slow</td>
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<td>Inter-die process variations</td>
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<td>Life-time degradation (NBTI, TDDDB)</td>
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<td>Intra-die process variations</td>
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<tr>
<td>Global</td>
<td>Slow-Changing</td>
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<td>Package/Die VDD fluctuations</td>
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<td>Ambient temperature variations</td>
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<td>Local IR Temperature hot-spots</td>
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<td>Capacitive Coupling Clock-tree jitter</td>
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<td>Fast-Changing</td>
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<td></td>
<td>PLL jitter</td>
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<td>IR drop</td>
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<td>Ldi/dt</td>
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</tbody>
</table>

[Bull, JSSC, Jan 2011]
All transistors within a chip see the same parameter values.

However these vary for different chips across a wafer, lots etc.
Correlated local: gates and transistors within a given local region see same variation.

Random Local: transistor to transistor and hence gate to gate variation
Ageing: NBTI, PBTI

NBTI: Prolonged negative gate bias increases $V_{th}$ over time
   PMOS typically operates in this regime

PBTI: Prolonged positive gate bias increases $V_{th}$ over time
   NMOS typically operates in this regime
   Becoming important in sub-45nm nodes.

Impact on delay?
$V_{\text{supply}}$ Variations

[Anirudh Devgan, IBM, Mar 05]
Temperature Variations

[Anirudh Devgan, IBM, Mar 05]
Fast fluctuations

PLL Jitter
Ldi/dt
IR Drop
Cap coupling
Clock-tree jitter
Dynamic/Adaptive Voltage Scaling

How to make the critical Path model?

Kaenel, JSSC Oct 1990
CPM Speed should track the DUT speed over all PVT with a small constant overhead.
Ring oscillator

Easy to measure delay (frequency measurement)

Use in conjunction with DLL or PLL for real time adjustment

Measure during manufacturing test to adjust bios rom etc.

Small area over head – can distribute across region
  Over come local variations (correlated)

Design with margins for
  Random local, Dynamic variations,
  Aging degradations
Delay Measurement

Ref. Clock
Detect Pulse
Delay of Delay Synthesizer
Detect Clock

Convert to Binary Data
Delay gap to target can be attained as a numerical value

Ref. Clock
Pulse Gen.
Detect Pulse
Delay Synthesizer
Detect Clock
Delay Line Element
Delay Line Gauge
Encoder
Target Point
Target value

Nakai, JSSC Jan 2005
Drake's CPM and edge detector

5 delay paths

Combination of two can be done to pick different ones across different supply Ranges.

Timing slack is current edge position from target edge position for DUT failure.

[Drake, et. Al, ISSCC 2007]
Delay comparison

[Drake, et. Al, ISSCC 2007]
Bit position at failure frequency.
Ideally CPM should have constant bit position. This has a spread of 3 bit locations. Can use linear interpolation.
Performance of DVC

Without Delay Synthesizer Circuit

With Delay Synthesizer Circuit

Nakai, JSSC Jan 2005
Activity monitor

Nakai, JSSC Jan 2005
Frequency decision flow chart

Activity Measurement

- If Frequency is greater than Effective Frequency + Margin, then:
  - If Frequency - Step is less than Effective Frequency + Margin, then hold frequency constant.
  - Otherwise, increase frequency by Step.

- Otherwise, decrease frequency by Step.
Clock control for DVFM

(1) Voltage Up by DFC
(2) Minimize Voltage by DVC
(3) Voltage Down by DFC

Reference Clock to DVC
System Clock
Voltage

(a) T

Reference Clock Freq. Up
System Clock Freq. Up
Both Clock Freq. Down

123MHz
96MHz
64MHz
48MHz
32MHz
24MHz
16MHz
8MHz

Thinned-out Clock Pulse

hazard free Clock Selector

System Clock

measured

Seamless frequency transition

24.5MHz
made of 32MHz
48.5MHz
made of 64MHz
Clock thinner

Clock Selecter

Counter

Decoder

Comp.

clk out
Thank You!