

SUPPORT FOR

SupportNet English Questa ADMS

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What is a path to POWER or GROUND in PATHCHK?



SYMPTOMS

What is a path to POWER or GROUND for the PATHCHK command?

TECHNOTE ID

MG76396

TECHNOTE TYPE

Reference

UPDATED

07 Dec 2012

PRODUCTS

Calibre nmLVS

Solution

The default ERC path is any path that leads through source/drain pins of MOS devices, and/or pos and neg pins of resistor devices.

The following 4 examples illustrate how PATHCHK finds a path to POWER or GROUND through source/drain pins of MOS devices.

For each example these rule statements apply:

```
LVS POWER NAME vdd
```

```
LVS GROUND NAME vss
```

The following shows paths to vdd POWER for all gates of pmos devices (pgate)



The following shows gates of pmos devices that do NOT have paths to vdd POWER



The following shows paths to vss GROUND for all gates of pmos devices (pgate)



The following shows gates of pmos devices that do NOT have paths to vss GROUND



The ERC definition of "path" can be modified by using the ERC PATH ALSO specification statement. This statement adds device pins to the definition of the ERC path.