Fast Decoders

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Hierarchical Word Line Architecture
Skewed Gates

**Inverter**

- **Unskewed**
  - $g_u = 1$
  - $g_d = 1$
  - $g_{avg} = 1$

- **HI-skew**
  - $g_u = 5/6$
  - $g_d = 5/3$
  - $g_{avg} = 5/4$

- **LO-skew**
  - $g_u = 4/3$
  - $g_d = 2/3$
  - $g_{avg} = 1$

**NAND2**

- **Unskewed**
  - $g_u = 4/3$
  - $g_d = 4/3$
  - $g_{avg} = 4/3$

- **HI-skew**
  - $g_u = 1$
  - $g_d = 2$
  - $g_{avg} = 3/2$

- **LO-skew**
  - $g_u = 2$
  - $g_d = 1$
  - $g_{avg} = 3/2$

**NOR2**

- **Unskewed**
  - $g_u = 5/3$
  - $g_d = 5/3$
  - $g_{avg} = 5/3$

- **HI-skew**
  - $g_u = 3/2$
  - $g_d = 3$
  - $g_{avg} = 9/4$

- **LO-skew**
  - $g_u = 2$
  - $g_d = 1$
  - $g_{avg} = 3/2$
Precharge based dynamic gate

(a)  

(b)  

(c)
Two Phased Operation

Footed

Unfooted

Precharge

Evaluate

Precharge
Logical Efforts of dynamic Gates

- **Inverter**
  - Unfooted: $g_d = 1/3$, $p_d = 2/3$
  - Footed: $g_d = 2/3$, $p_d = 3/3$

- **NAND2**
  - Unfooted: $g_d = 2/3$, $p_d = 3/3$
  - Footed: $g_d = 3/3$, $p_d = 4/3$

- **NOR2**
  - Unfooted: $g_d = 1/3$, $p_d = 3/3$
  - Footed: $g_d = 2/3$, $p_d = 5/3$
Dynamic Decoder
Keeper
Fast Predecoder

\[ Y = ABCD \]

Dynamic NOR

Domino Buffer
Power Dissipation

• Dynamic Style for the entire decoder
  – Leads to excessive clock power
    • Distribute the clock to all the word line and gates
Post Charge Gates

Reset Chain

[Amrutur, et. al., JSSC 2001]
Delayed Reset CMOS

Predicated Reset

weak

weak
Putting it all together