Layout Basics

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Basic Design Rules
Standard Cells

(a) 
(b) 
Substrate Tap

Well Tap

V_{DD}

GND

4 \lambda

32 \lambda

40 \lambda
Wells and contacts

(a) Substrate Contact  n transistor  Gate Extension  p transistor  Well Contact

(b) Substrate Contact  n transistor  Gate Extension  p transistor  Well Contact
Substrate contact
Geometry operations

\textbf{AND} \ (layer1 \ and \ layer2) \rightarrow \ layer3
\begin{itemize}
  \item ANDs \ layer1 \ and \ layer2 \ together \ to \ produce \ layer3 \\
  \item (i.e., \ the \ intersection \ of \ the \ two \ input \ mask \ descriptions)
\end{itemize}

\textbf{OR} \ (layer1 \ or \ layer2) \rightarrow \ layer3
\begin{itemize}
  \item ORs \ layer1 \ and \ layer2 \ together \ to \ produce \ layer3 \\
  \item (i.e., \ the \ union \ of \ the \ two \ input \ mask \ descriptions)
\end{itemize}

\textbf{NOT} \ (layer1 \ minus \ layer2) \rightarrow \ layer3
\begin{itemize}
  \item Subtracts \ layer2 \ from \ layer1 \ to \ produce \ layer3 \\
  \item (i.e., \ the \ difference \ of \ the \ two \ input \ mask \ descriptions)
\end{itemize}

\textbf{WIDTH} \ (layer \ > \ dimension) \rightarrow \ layer3
\begin{itemize}
  \item Checks \ that \ all \ geometry \ on \ layer \ is \ larger \ than \ dimension \\
  \item Any \ geometry \ that \ is \ not \ is \ placed \ in \ layer3
\end{itemize}

\textbf{SPACE} \ (layer \ > \ dimension) \rightarrow \ layer3
\begin{itemize}
  \item Checks \ that \ all \ geometry \ on \ layer \ is \ spaced \ further \ than \ dimension \\
  \item Any \ geometry \ that \ is \ not \ is \ placed \ in \ layer3
\end{itemize}
DRC Checking

nwell
  NOT  all nwell -> substrate
active
  AND  nwell active -> nwell-active
n-select
  NOT  active nwell -> pwell-active
poly
  AND  nwell-active p-select -> pdiff
poly-contact
  AND  nwell-active n-select -> vddn
active-contact
  AND  pwell-active n-select -> ndiff
metal
  AND  pwell-active p-select -> gndp

  AND  poly ndiff -> ngates
  AND  poly pdiff -> pgates

WIDTH  metal  < 0.13  ->  metal-width-error
SPACE  metal  < 0.13  ->  metal-space-error
Antenna Rule

Long metal1 connected to gate can cause damage.

Add metal2 jumper to fix problem.

Add diode to fix problem.
Yield enhancement guidelines

- Space out wires to reduce risk of short circuits and reduce capacitance.
- Use non-minimum-width wires to reduce risk of open circuits and to reduce resistance.
- Use at least two vias for every connection to avoid open circuits if one via is malformed, and to reduce electromigration wearout.
- Surround contacts and vias by landing pads with more than the minimum overlap to reduce resistance variation and open circuits caused by misaligned contacts.
- Use wider-than-minimum transistors; minimum-width transistors are subject to greater variability and tend not to perform as well.
- Avoid non-rectangular shapes such as 45-degree angles and circles. For specialized circuits such as RAMs that strongly benefit from 45-degree angles, verify masks after optical proximity correction analysis.
- Place dummy transistors or cells at the edge of arrays and sensitive circuits to improve uniformity and matching.
- If it looks nice, it will work better.