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On-Chip Clock Network Skew Measurement using Sub-Sampling

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***Abstract*—We present a technique for an all-digital on-chip delay measurement system to measure the skews in a clock distribution network. It uses the principle of sub-sampling. Measurements from a prototype fabricated in a 65 nm industrial process, indicate the ability to measure delays with a resolution of 0.5ps and a DNL of 1.2 ps.**

I. Introduction

Modern synchronous chips use large clock distribution networks spread over the entire die to distribute the clock to hundreds of thousands of sequential elements. The relative arrival time difference between clock signals at the leaf nodes of this distribution network, the clock skew, directly eats into the timing margins [1]. Hence elaborate care is taken to design these distribution networks, to minimize this skew. However, random within-die variations, along with other un-modeled systematic variations still introduce a residual skew in the network. Hence a technique to measure the relative skew between two arbitrary leaf nodes of the clock network in situ will be of great value in studying and characterizing the skews as well as potentially enabling a closed loop design of the clock network to reduce the skew.

Techniques to measure skew between two signals are well known and routinely used in Phase Lock Loops (PLL), Delay Lock Loops (DLL) and Time-to-Digital Converters [2-5]. PLLs and DLLs use a phase detector followed by a filter which gives a measure of the relative skew between two periodic signals. The authors in [3] propose a very precise coarse-fine time-to-digital converter which multiplies time residue for improving the timing resolution. The authors in [4] propose a flash Time-to-Digital converter which utilizes arbiters and can be calibrated for very high resolution. It uses the spread of arbiter threshold voltages for getting a set of digital codes from an array of arbiters to measure the delay. But it is limited by the non-uniform distribution of the offsets of the arbiters. The authors in [5] survey some of the popular digital techniques for delay measurements which use tapped and vernier delay line methods. While the phase detector based approach works only with periodic signals, some of the other time digitization techniques also work for non-periodic signals. However, all these techniques are difficult to use to measure the skew between two leaf nodes with arbitrary physical separation. This is because it becomes difficult to route these signals from the leaf nodes of the network to a common measurement location without adding any extra skew, thus corrupting the measurement. Nevertheless, for leaf nodes which are physically close by, phase detectors followed by filters have been used in the active de-skew scheme by the authors in [2]. Alternative techniques like the PICA method or SEM imaging can be used to measure the clock skew of arbitrary leaf nodes [6]. However these sophisticated techniques require extensive physical modification of the die and package and are very expensive to use on a large scale. In this paper, we will explore a circuits-based approach to make the skew measurement across spatially distributed nodes. We take advantage of the periodic nature of the clock signal and apply the well known principle of sub-sampling.

We review this sampling technique and its application to distributed clock skew measurement in Section II. We discuss some of the limitations of the scheme and the implementation issues in Section III. We describe the measurement results from a test chip in Section IV followed by our conclusions in Section V.

II. Sub-Sampling for Distributed Clock Skew Measurement

When a periodic signal with period T, is sampled by another signal with a period $T + \Delta T$ where ΔT is small in comparison to T, the output of the sampler is a periodic beat signal with period $T/\Delta T * (T+\Delta T)$ (fig. 1). Such an approach has been used to monitor the internal signals within a chip in [7]. In a sense the time axis is expanded by a factor of $T/\Delta T$. As a corollary, if two signals each of period T, but separated by T_{skew} are sampled by a signal of period $T + \Delta T$, the two beat signals will be separated by $T_{skew} \times (T + \Delta T)/\Delta T$. Thus a small skew of T_{skew} can be amplified by a large factor and can be easily measured with digital techniques. By controlling the ratio $T/\Delta T$, one can obtain large amplifications and hence measure very small skews.

This principle can be used to make distributed clock skew measurement as shown in fig. 2. Here the triangle on the left side represents the clock distribution network of the main core clock to all its sequencing elements. In addition for a subset of the leaf nodes of this network, additional samplers are inserted at these locations, determined *a priori* during design time. The core clock is fed to the data input of these samplers and they are clocked by a separate sampling clock. The sampling clock is of a period which is slightly different from the core clock. The outputs of these samplers are of the beat period and are routed to a central measurement location for further analysis. Note that in this scheme, the core clock at the leaf nodes are minimally perturbed, thus preserving their original skews. Additionally, the routing of the beat signals to the central measurement unit needs to be done with a very relaxed timing constraint of a beat period. A

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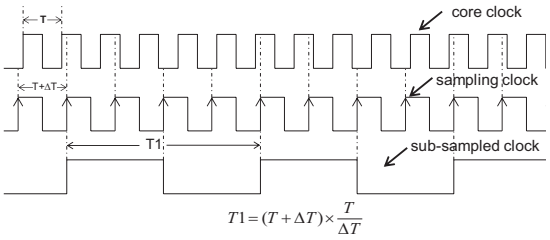

Figure 1. Illustration of sub-sampling system.

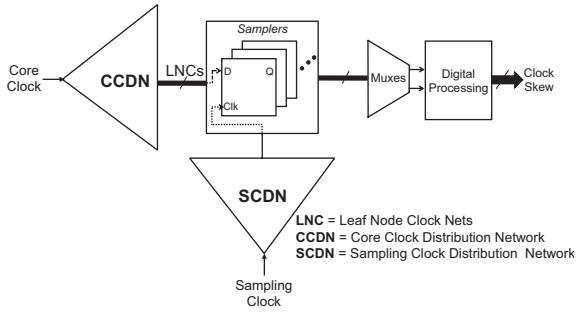

Figure 2. Illustration of the concept of skew measurement in a distributed clock network.

multiplexer can be used to select a pair of beat signals to determine their relative skews. Thus relative skews between all pairs of leaf nodes can be determined.

In this scheme the sampling clock needs to be distributed with ideally zero skew. But this is a much simpler problem, than of routing the original leaf node signals with matching skew constraints to a central location. The sampling clock network will have orders of magnitude lesser number of samplers (flops) and hence can be over designed to have very low skews. Existing clock tree synthesis tools can be used to complete the sampling clock network design, thus making it compatible with existing tool flows.

By observing the output waveforms from any leaf node, an estimate of the core clock edge occurrence can be obtained. Observations over many cycles will lead to better accuracy of this estimate. The estimates of the time of edge occurrence from two different leaves can then be subtracted to give an estimate of the average skew between the core clocks at the two leaf nodes.

With a zero skew SCDN the methods discussed in [3-5] can be used to measure the desired skew. However the entire measurement unit has to be embedded at each test node leading to large area and power overhead. In the proposed solution only a single digital sampler (flip-flop) is added at each node without making much change to the design flow, and hence is more practical.

III. Limitations and Implementation Issues

The beat signal period for any beat cycle will be an integral multiple of the sampling clock cycles, as the beat signal edges are triggered by the sampling clock edges. Thus even the relative skew between two leaf clock beat signals will be an integral multiple of sampling clock cycles. Because of the jitter in the core clock and the sampling clock, a single measurement of this relative skew will not suffice for accurate measurements and instead many measurements and averaging over these needs to be done. This puts the following constraints on the clocks and the skews:

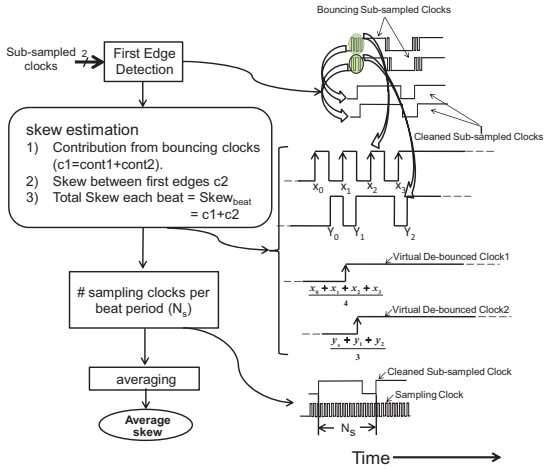

Figure 3. Digital processing for smaller ΔT.

1. The period of the core clock and sampling clock should be invariant over the measurement window.
2. The skew should change at a rate lower (by less than half) than the bandwidth of the measurement.

Any skews in the sampling clock or mismatches in the setup/hold time of the samplers will limit the measurement accuracy. By using larger sized transistors and ensuring good rise times in the sampling clock network, the effect of local mismatches can be reduced, as the random local variation reduces with size as $\frac{1}{\sqrt{width \times Length}}$ [8]. Monte Carlo simulations of a standard Master Slave Flip-flop with local within-die variation indicates maximum mismatch of 4 ps in the setup times at the rise time of 1 FO4 delay for the core and sampling clocks. But by using 2-3X larger sized transistors in the master stage of the DFF, the maximum variation reduces to within 1 ps. The authors in [9] have shown that by using the fine mesh distribution, a skew within 1 ps can be achieved. A similar technique can be applied for the SCDN, and since the number of nodes is small, it can be implemented with much less impact on total power.

Smaller skews can be resolved by using a small ΔT as large amplifications can be achieved. Interestingly, the resolution of the system is not limited by ΔT, i.e. skews even smaller than ΔT can be measured. This is because the inherent jitter helps in obtaining enough samples over a large measurement window to help determine these smaller than ΔT skews.

However jitter coupled with small ΔT leads to bouncing in the beat signal near its transition edges (fig. 3) due to some instantaneous negative values of ΔT. To take care of this, a cleaned version of the sub-sampled signals is generated as shown in the fig. 3. Various de-bouncing algorithms are possible. A simple de-bouncing technique is to use the first rising edge of the bouncy signal as the rising edge of the de-bounced signal. However an isolated bounce due to a momentary high or low (negative) value of ΔT or metastability can lead to inaccuracies in the skew measurement. To solve this problem we first determine the rising edges of (virtual) de-bounced clocks by averaging over the rising edges of the bounced clocks and then measure the delay between the rising edges of these de-bounced clocks.

De-bouncing Algorithm

1. Detect the first rising edges of both the bouncing sub-sampled clocks in each beat and find the delay between them.
   This delay is given by $Y_0 - X_0$ in fig. 3.
   The output of first edge detect circuit is made of around 75% duty cycle to avoid false triggering within a beat by the rising edges corresponding to the falling edge glitches of bouncing sub-sampled clocks.
2. Estimate the contribution from the bouncing edges for both the bouncing clocks towards the total time amplified skew in each beat.
   This is given by $-(\sum_{i=1}^{3}\frac{X_i - X_0}{4})$ for sub-sampled clock1 and $\sum_{j=1}^{2}\frac{Y_j - Y_0}{3}$ for sub-sampled clock2 in fig. 3.
3. Estimate the time amplified skew per beat which is obtained by adding the delays obtained in step1 and step2.
   Referring to fig. 3, this is given by
   $$Delay\ count\ per\ Beat = \sum_{j=0}^{2}\frac{Y_j}{3} - \sum_{i=0}^{3}\frac{X_i}{4}\ .$$
4. Estimate the no. of sampling clocks per beat period (N_s).
5. Find
   $$R_{beat} = \frac{\text{Delay count per Beat}}{\text{Sampling Clocks per Beat}}.$$
   Taking this ratio reduces the error introduced due to any continuous trend of higher or lower values of ΔT over a period of time as in that case both the numerator and denominator will be simultaneously high or low.
6. Find the estimate of R_{beat} for 2^n samples ($\mathbb{E}[R_{beat}]$) where minimum value n will depend upon the tolerance bound and the relative jitter specs of the clocks. Knowing the spread of R_{beat}, Hoeffding's inequality [10] can be applied to estimate the minimum value of n, which was found to be 17 in our case (i.e. average over 2^{17} samples were taken.)
7. Find $\frac{\mathbb{E}[\mathbf{R_{beat}}]}{f_{core\_clk}}$.
   f_{core_clk} is the core clock frequency.

This estimate is nothing but the estimate of input skew referred from the time amplified sub-sampled signals.

The choice of ΔT (the difference in time periods of the core clock and sampling clock) affects the accuracy of measurement in the form of time amplification, measurement time and "amount of bounce" of the beat signals.

IV. Experimental Results

A test chip was fabricated in a 65nm process node (fig. 4). The test structure essentially consisted of a number of samplers, and the multiplexer. The two leaf clock inputs were supplied from outside so that calibrated skews could be provided and the performance of the technique could be studied. Similarly, the sampling clock was also provided

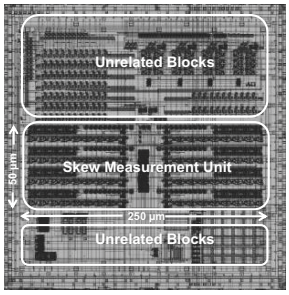

Figure 4. Chip layout of the skew measurement unit in 65nm CMOS Process.

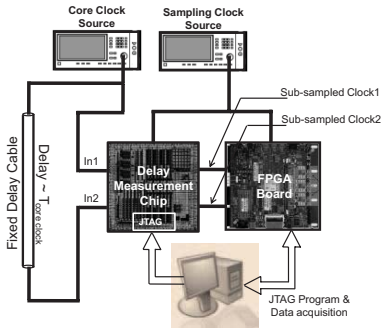

Figure 5. Measurement setup in the lab.

from outside. The beat signal outputs from the multiplexers were directly taken out of the chip, so that various de-bouncing algorithms and digital processing options could be experimented with in a flexible manner. The lab setup for our experiments is shown in fig. 5. Two clock sources provide the core and sampling clocks. The core clock is split and one of the paths is taken through a cable of fixed delay, to provide the two leaf clock inputs to the DUT. The beat output of the DUT is fed to a FPGA board where further processing is done to extract the input skews. Since we did not have signal generators which could generate two leaf clocks with pico-second resolution delays, we synthesize such delays using a cable of fixed length, and varying core clock frequency. When the clock period is about the same value as the cable delay, then the relative delays between the edges at the input and output of the cable can be adjusted by adjusting the clock period (fig. 6).

Since it is easy to obtain precise frequency sources, we could obtain precise pico-second level delay inputs to the DUT. The measured skews by this technique as a function of input skews are shown in fig. 7. The input delays are changed in steps of 1.1 ps by varying the frequency of the core clock. The DNL (maximum error) is found to be 1.2 ps. As shown in fig. 8, at the ΔT value of 1.1 ps, the output delay was very erroneous and also at a higher ΔT of 5.5 ps there was a loss of monotonicity for the input delay of 5.5 ps. Hence, the period difference between the core clock and sampling clock, ΔT, was chosen to be 3.3 ps. For the same input delay, multiple measurements were done for the output delay, and the maximum spread between these measurements was found to be within 0.5ps. These variations can be attributed to various factors like drift in the frequency of the generators or even in the input delays to which our set up was very sensitive. Also it can be observed in fig. 7 that

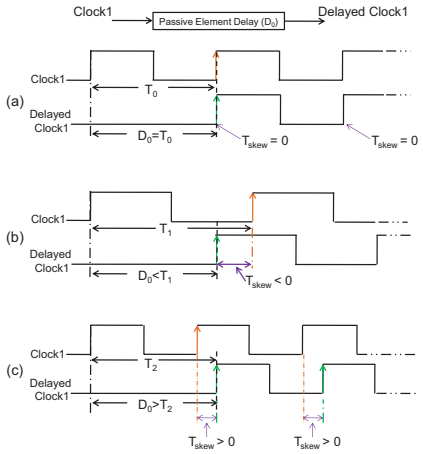

Figure 6. Setup for generation of precise delay steps.

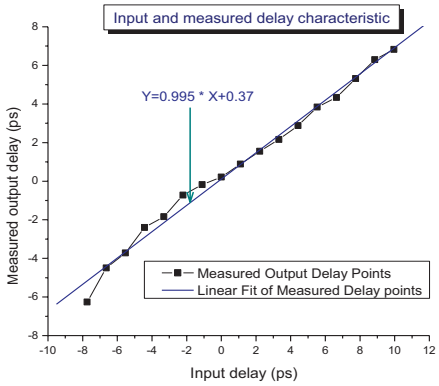

Figure 7. Input output delay characteristics.

even if the value of ΔT was chosen to be 3.3ps, skews less than 3.3ps were measured successfully due to the inherent jitter. Over the entire range of input delays, the output is monotonic. Hence the technique can also be used in the feedback system for skew compensation even for distributed leaf nodes. The area overhead of this technique consists of the extra samplers, the SCDN and the small amount of digital processing logic (≈5K NAND3 equivalent gates or 8000μm^2). The time to perform the experiment will depend upon the parameters like the choice of ΔT, no. of samples chosen etc. which will again depend on the relative stability of the clock sources. In our case, total number of samples chosen was around 100000 and the time taken for each measurement was $\approx \frac{10^5}{\Delta T * core\ clock\ frequenc\ y^2} \approx 25$ seconds for a core clock frequency of 35 MHz. The frequency is limited by our experimental setup. But we believe, this technique is applicable to any clock frequency, as the sub-sampling principle works for any frequency.

V. Conclusion

The sub-sampling technique enables on-chip skew measurement between two leaf nodes of a clock distribution network which are physically far apart. Instead of sending the leaf node signals with strict matching requirements to a central measurement unit, another clock source with much less loading needs to be distributed with low skews to

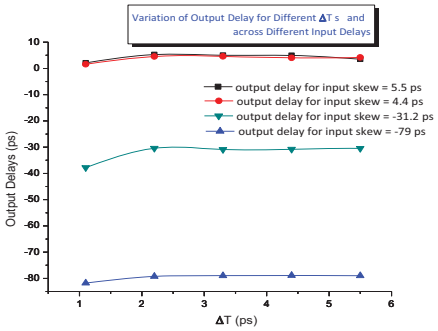

Figure 8. Sensitivity of measured delay to ΔT.

routed to a central processing unit which can digitally measure the skews. Combined with the clock generation technique from [7], a fully monolithic implementation can be achieved. Through a mux structure the sub-sampled signals from any two arbitrary nodes in a clock tree can be selected and routed to the central processing unit thus accommodating the measurement over a large number of leaf nodes. The selection of the period difference between the two clock sources needs to balance the measurement time and accuracy. Skews even smaller than the period differences (ΔT) can be measured due to the inherent jitter in the clocks and the averaging aspect of the measurement technique. A prototype implementation demonstrates measurement accuracy to within 0.5ps and DNL of 1.2ps.

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References

[1] E. G. Friedman, "Clock distribution networks in synchronous digital integrated circuits," *Proceedings of the IEEE*, 89(5):665--692, May 2001.

[2] P. Mahoney et al., "Clock distribution on a dual-core, multi-threaded Itanium®-family microprocessor," *ISSCC Dig. Tech. Papers*, 2005, pp. 292-293.

[3] M. Lee, A.A. Abidi, "A 9b, 1.25ps resolution coarse–fine time-to-digital converter in 90nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, Vol.43, no.4, April. 2008.

[4] V. Gutnik, A. Chandrakasan, "On-chip pico second time measurement," *Symposium on VLSI Circuits Dig. Tech. Papers*, Apr. 2000.

[5] M.A. Abas et al., "Built-in time measurement circuits – a comparative design study," *Computers & Digital Techniques, IET Symposium on VLSI Circuits Dig. Tech. Papers*, Vol.1, no. 2: 87-97 March. 2007.

[6] P.N. Sanda et al., "Picosecond imaging circuit analysis of the power3 clock distribution," *ISSCC Dig. Tech. Papers*, 1999, pp. 372-373.

[7] Y. Zheng, K.L. Shepard, "On-chip oscilloscopes for noninvasive time-domain measurement of waveforms in digital integrated circuits," *IEEE Tran. on VLSI*, Vol.11, no.3, June. 2003.

[8] F. Arnaud et al., "Low Cost 65nm CMOS platform for low power & general purpose applications," *Symposium on VLSI Circuits Dig. Tech. Papers*, June. 2004, pp. 10-11.

[9] C. Yeh et al., "Clock distribution architectures: a comparative study" in *Int.Symp. Quality Electronic Design (ISQED) Dig. Tech. Papers*, March 2006.

[10] W. Hoeffding, "Probability inequalities for sums of bounded random variables," *J. American Statistical Association,* Vol. 58, no.301: 13–30, March 1963.